A Micropower Log-Domain Filter Using Enhanced Lateral PNPs in a 0.25 μm CMOS Process

N. Krishnapura[1], Y. Tsividis[2]
[1]Celight Inc., 485 D Route 1 South, Iselin, NJ, 08830, USA.
[2]Dept. of EE, Columbia University, New York, NY, 10027, USA.

Abstract

A 2^{nd} order low-pass log-domain filter is fabricated in a 0.25 μm CMOS technology using enhanced lateral bipolar transistors. pMOS devices operating in accumulation are used for the integration capacitors. The filter, when tuned to a bandwidth of 22 kHz, consumes 4.1 μW from a 1.5 V supply and has an rms output noise of 0.25 nA. The filter's *SNR* at 1% *THD* is 56.1 dB and its maximum $S/(N+THD)$ is 44.9 dB. The chip occupies 0.085 mm^2.