Bit Line Coupling Scheme and Electrical Fuse Circuit For Reliable Operation of High Density DRAM

Kyunam Lim, Sangseok Kang, Jonghyun Choi, Jaehoon Joo, Younsang Lee, Jinseok Lee, Sooin Cho, Byungil Ryu

DRAM Design 1, Memory Product and Technology Division, Samsung, Korea

San 24 Nongseo-Ri, Kiheung-Eup, Yongin, Kyunggi-Do, 449-711, Korea

Two design techniques are presented to improve the yield of high density DRAM product. One is Bit Line Coupling(BLC) scheme and the other is Electrical Fuse(E-Fuse) circuit for reliable field programmable repair scheme. We obtain an improvement of 100ms for the data retention time(tREF) using the BLC scheme. BLC scheme also improves the low VCC margin by 0.3V and the RAS to CAS delay time(tRCD) by 1.5ns. Differential current evaluation for the E-fuse implementation shows polysilicon fuse fail rate $< 10^{-12}$.