

A 66-400 MHz, Adaptive-Lock-Mode DLL Circuit with Duty-Cycle Error Correction

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A DLL circuit featuring variable “lock mode” and correction of duty-cycle error is described. The DLL has a locking range from under 66 MHz to 400 MHz. The DLL automatically changes its lock mode according to the current clock frequency and corrects the duty-cycle error so that the phases of the both edges match those of the external clocks. The chip area and power consumption at 400 MHz are 0.33 mm² and 24 mW, respectively.