

This paper describes a custom design method of ASICs with on-demand library generation. According to the result of performance estimation, a tailored library is generated and supplied to cell-based design tools. A symbolic layout system that produces a cell layout with variable driving strength is developed. The tunability can be utilized for generating a rich set of driving strength as well as design optimization in post-layout stage. Design experiments and measured performance of a fabricated chip demonstrate the effectiveness of the proposed approach.