

Scaling Scenario of Multi-level Interconnects for Future CMOS LSI

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The scaling guidelines of the multi-level interconnects for future CMOS LSI are presented. It is based upon intensive circuit simulation combined with 2D field solver while considering wire length distribution of logic circuits. Interconnect structures such as metal aspect ratio and ILD thickness are optimized to minimize wiring delay without causing crosstalk problem. Furthermore, the scaling trend of BEOL parameters are presented.