

Highly Manufacturable and High Performance SDR/DDR 4Gb DRAM

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Abstract

A 4Gb SDR/DDR DRAM is fabricated with 0.11 μm CMOS technology. To the best of our knowledge, this is the first working highest density DRAM ever achieved. The cell size and the chip size of 4Gb DRAM are approximately 0.1 μm^2 and 645 mm^2 , respectively. In order to achieve highly manufacturable and high performance 4Gb DRAM, constraints imposed by extremely small cell size and large chip size should be overcome. We have found that random single-bit and/or twin-bit failures and block failures are the most critical issues to be solved for achieving good functionality of 4Gb DRAM. In order to get rid of the single and twin bit failures, *80nm array transistor, sub-80nm memory cell contact and mechanically robust capacitor* are developed. In order to remove block failure and at the same time achieve high performance, *triple-level CVD Al BEOL* technology is developed. These technologies for achieving good functionality with high performance have good compatibility for previous generation as well as excellent extendibility for next generations.