

Scaling Towards 35nm Gate Length CMOS

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Summary

We report 35nm gate length planar CMOS transistors with aggressively scaled gate equivalent oxide thickness (EOT). Nitride / oxynitride (N/O) stack was used as gate dielectric with EOT ranging from 12Å down to 7Å. The impact of gate scaling on transistor performance, gate tunneling leakage, short-channel effect, and channel carrier mobility is investigated. Excellent control of short-channel effect is achieved for sub-50nm gate length devices. CV/I delays of 0.89ps for n-MOSFET and 1.8ps for p-MOSFET are demonstrated at a supply voltage of 0.85V.