Shallow n^+/p^+ junction formation using plasma immersion ion implantation for CMOS Technology

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We present CMOS transistors with n^+/p^+ source/drain extensions doped by AsH_3 and BF_3 plasma immersion ion implantation (PIII) for the first time. We successfully demonstrate n^+/p^+ shallow junctions with $R_s < 1$ kΩ/sq for CMOS devices. No degradation in gate oxide integrity is observed for either AsH_3 or BF_3 PIII. Compared to conventional ion implantation, PIII provides much better short-channel effects and approximately 50% I_{OFF} reduction for both nMOS and pMOS devices. In particular, the flat threshold voltage roll-off and good performance in buried-channel pMOS device is the best-reported PIII data to date.