

75 Word Abstract

Carrier Mobility Enhancement in Strained Si-On-Insulator Fabricated by Wafer Bonding

L.-J. Huang, J.O. Chu, S.A. Goma, C.P. D'Emic, S. J. Koester, D. F. Canaperi, P. M. Mooney,
S. A. Cordes, J. L. Speidell, R. M. Anderson, H-S Philip Wong

IBM Thomas J. Watson Research Center

Yorktown Heights, NY 10598, USA

N- and p-MOSFETs have been fabricated in strained Si on SiGe on insulator (SSOI) with high (15%-25%) Ge content. Wafer bonding and H-induced layer transfer techniques enabled the fabrication of the high Ge content SiGe-On-Insulator (SGOI) substrates. Mobility enhancement of 50% for electrons (with 15% Ge) and 15%-20% for holes (with 20%-25% Ge) has been demonstrated in SSOI MOSFETs. This could lead to the next generation device performance enhancement.