Novel Damage-free Direct Metal Gate Process Using Atomic Layer Deposition

Dae-Gyu Park, Kwan-Yong Lim, Heung-Jae Cho, Tae-Ho Cha, Joong-Jung Kim, Jung-Kyu Ko, In-Seok Yeo, and Jin Won Park

Advanced Process Team, Memory R&D Division, Hyundai Electronics Industries Co. Ltd., Ichon P.O. Box 1010, Ichon-si, Kyoungki-do, Korea 467-701 (E-mail: dpark@sr.hei.co.kr)

We report novel characteristics of W/TiN/SiO_2/p-Si *n*MOS system using atomic layer deposition (ALD)-TiN. Damage-free direct metal gate was attained with ALD-TiN as manifested by the negligible hysteresis and low interface trap density (D_{it}) as low as ~$5x10^{10}$ $eV^{-1}cm^{-2}$ near the Si midgap. In addition, ALD-TiN demonstrated remarkable reduction of gate leakage current and highly robust gate oxide reliability with negligible capacitance equivalent thickness variation against high thermal budget, paving a way for the direct metal gate process.