Scalability and Biasing Strategy for CMOS with Active Well Bias

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Abstract

We analyze the scalability of the two well bias strategies: reverse bias to reduce standby power, and forward bias to improve the speed or to reduce active power. We then present the device design space that includes well bias as an integral part of the design variables following the SIA Roadmap specifications. We show that proper well biases are needed for bulk CMOS just to continue to meet the SIA Roadmap requirements for performance and standby current. The scalabilities for forward bias and reverse bias are different. The advantage of reverse bias is diminishing with scaling due to low initial V_t values, short-channel effect, and band-to-band tunneling. The advantage of the forward body bias is preserved better with scaling due to high initial V_t values as well as smaller depletion width, and increases with V_t non-scaling. The forward bias approach is not effective in speed improvement for ultra-high performance applications with high V_{dd} overdrive and low V_t to start with, but is effective in active power reduction at a fixed speed target.