Dual Supply Voltage Clocking for 5GHz 130nm Integer Execution Core

Ram K. Krishnamurthy, Steven Hsu, Mark Anders, Brad Bloechel, Bhaskar Chatterjee*, Manoj Sachdev*, Shekhar Borkar

Circuits Research, Intel Labs, Intel Corporation, Hillsboro, OR 97124, USA, ramk@ichips.intel.com

*University of Waterloo, Ontario N2L3G1, Canada, bhaskar@vlsi.uwaterloo.ca

This paper describes dual- V_{cc} clocking on a 1.2V, 5GHz integer execution core fabricated in 130nm CMOS to achieve up to 71% measured clock power (including 15% active leakage) reduction. A write-port style pass-transistor latch and split-output level-converting local clock buffer are described for robust, DC power free low- V_{cc} clock operation.