

## **A 4.5GHz 130nm 32KB L0 Cache with a Self Reverse Bias Scheme**

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This paper describes a 32KB dual-ported L0 cache for 4.5GHz operation in 1.2V, 130nm CMOS. The local bitline uses a Self Reverse Bias scheme to achieve  $-220\text{mV}$  access transistor underdrive without external bias voltage or gate-oxide overstress. 11% faster read delay and 104% higher DC robustness (including 7x measured active leakage reduction) is achieved over optimized high-performance dual-Vt scheme.