Static Pulsed Bus for On-Chip Interconnects

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A Static Pulsed Bus (SPB) technique offers significant advantages over conventional static bus (SB) in delay, energy, total device width and peak V_{CC} current for 1500μm to 4500μm long M4 buses in a 100nm technology. These improvements are due to reduction in effective coupling capacitance and repeater skewing enabled by monotonic signal transition. Unlike dynamic schemes, energy savings of SPB are maintained across all activity factors without any clock power or routing overhead.