A 5Gbps CMOS Frequency Tolerant Multi Phase Clock Recovery Circuit

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A Clock and Data Recovery (CDR) circuit using Multi Phase Gated VCO (MGVCO) technique for multi-channel high-speed serial interface was developed. The MGVCO architecture can realize high-speed CDR operation, quick data acquisition and plesiochronous clocking capability. To verify effectiveness of the architecture, 5Gbps 32-channel testchip was fabricated in 0.18μm CMOS technology. BER of $<10^{-12}$ with +/-3% frequency tolerance in 5Gbps CDR operation for random incoming data of 2^7-1 was measured with small channel location dependency.