A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slew-rate-controlled output buffer

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We developed a 1-Gb/s/pin 512-Mb DDRII SDRAM composed of a digital delay-locked loop (DLL) and a slew-rate-controlled output buffer. The digital DLL has a frequency divider for the DLL input, which performs at a operating frequency of up to 500 MHz at 1.6 V, and it provides internal clocking with 50% duty-cycle correction. The DLL has a current-mirror-type interpolator, which enables a resolution as high as 14 ps, is standby-current-free, and can operate at voltages as low as 0.8 V. The slew-rate impedance-controlled output buffer circuit reduces the output skew from 107 to 10 ps. This SDRAM was tested using a 0.13-um 126.5-mm^2 512-Mb device.