1-Gb/s/pin Multi-Gigabit DRAM Design with Low Impedance Hierarchical I/O Architecture

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Abstract

A low impedance hierarchical I/O architecture designed to realize both high-speed and low-voltage DRAMs is presented. In this architecture, use of the divided I/O lines over the memory cells reduces the load of I/O lines by 50% and enables a 2.2 ns reduction of the read/write cycle time. By combining distributed data transfer scheme, we achieved a 4 ns reduction of the access time to 8 ns and 1-Gb/s/pin operation with a 1.8-V power supply in a multi-Gb DRAM.