<100> Channel Strained-SiGe p-MOSFET with Enhanced Hole Mobility and Lower Parasitic Resistance

M. Shima, T. Ueno, T. Kumise, H. Shido, Y. Sakuma, and S. Nakamura FUJITSU LABORATORIES LTD 10-1 Morinosato-Wakamiya, Atsugi 243-0197, Japan Tel: +81-462-50-8237 Fax: +81-462-48-3473 E-mail: mashima@flab.fujitsu.co.jp

 $\label{eq:employment} Employment of <100> channel direction in a strained-Si_{0.8}Ge_{0.2} p-MOSFET has demonstrated the substantial amount of hole mobility enhancement as large as 25% and parasitic resistance reduction of 20% compared toa <110> strained-Si_{0.8}Ge_{0.2} channel p-MOSFET, which already has an advantage in mobility and the threshold voltage roll-off characteristic over the Si p-MOSFET. This result indicates that the <100> strained SiGe channel p-MOSFET is a promising and practical candidate for realizing high-speed CMOS devices under low-voltage operation.$