High Performance CMOS Operation of Strained-SOI MOSFETs using Thin Film SiGe-on-Insulator Substrate

T. Mizuno, N. Sugiyama, T. Tezuka, T. Numata, and S.Takagi

MIRAI Project, Association of Super-Advanced Electronics Technology (ASET)
1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki, Japan 212-8582 (mizuno@amc.toshiba.co.jp)

We have demonstrated, for the first time, high performance CMOS operation of FD and PD strained-SOI MOSFETs on a new thin-film-SGOI substrate with high Ge content (25%) fabricated by the combination of SIMOX and ITOX technologies, without using usual thick SiGe buffer layers. Actually, we have verified large electron (85%) and hole (50%) mobility enhancement of strained-SOI MOSFETs, against the universal carrier mobility. It is demonstrated, as a result, that the gate delay time of strained-SOI CMOS is improved by about 70%, compared to that of control-SOI CMOS. Moreover, we have also shown that only hole mobility enhancement depends on both the strained-Si thickness and the effective field in strained-SOI CMOS.