Lithography Solution for 65-nm Node System LSIs

Takahiro Matsuo, Masayuki Endo, Shinji Kishimura, Akio Misaka and Masaru Sasago

ULSI Process Technology Development Center, Semiconductor Company,

Matsushita Electric Industrial Co., Ltd.

19, Nishikujo-Kasugacho, Minami-ku, Kyoto 601-8413, Japan

Phone : +81-75-662-8994, Fax : +81-75-662-8995, E-mail : matsuo@krl.mec.mei.co.jp

Abstract

For 65-nm node devices, we have systematically investigated the lithographic margin of the electron-beam projection lithography (EPL), ArF lithography and vacuum ultraviolet (VUV) lithography. Among them, EPL has sufficient margin and excellent pattern fidelity and our experiments have demonstrated that it can fabricate 65-nm node device patterns. Therefore, EPL is a strong candidate for 65-nm node lithography.