

# Self-Aligned Ultra Thin HfO<sub>2</sub> CMOS Transistors with High Quality CVD TaN Gate Electrode

C. H. Lee, J. J. Lee, W. P. Bai, S. H. Bae, J. H. Sim, X. Lei<sup>\*</sup>, R. D. Clark<sup>\*</sup>, Y. Harada<sup>\*\*</sup>, M. Niwa<sup>\*\*</sup> and D. L. Kwong  
Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas, Austin, TX 78758  
<sup>\*</sup>Schumacher, Calsbad, CA 92009, <sup>\*\*</sup> Matsushita, Kyoto, 601-8413, Japan

In this paper, we have demonstrated and characterized self-aligned, gate-first CVD TaN gate n- and p-MOS transistors with ultra thin (EOT=11~12Å) CVD HfO<sub>2</sub> gate dielectrics. These transistors show no sign of gate deletion and excellent thermal stability after 1000°C, 30s N<sub>2</sub> anneal. Compared with PVD TaN devices, the CVD TaN/HfO<sub>2</sub> devices exhibit lower leakage current, smaller CV hysteresis, superior interface properties, higher transconductance, and superior electron and hole mobility.