

Study of Substrate Noise and Techniques for Minimization

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Abstract

This paper presents a study of substrate noise effects on analog circuits and a technique for minimizing substrate noise. Measured data of a 0.25 μ m CMOS test chip reveals that substrate noise couples through circuit asymmetries and nonlinearity, degrading analog circuit performance. An active substrate noise shaping circuit implemented on the same test chip demonstrates over 10dB improvement in SNDR in the 0-20kHz band of a delta-sigma modulator for substrate noise generated by an inverter array.