3-Transistor Antifuse OTP ROM Array using Standard CMOS Process

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75 Word abstract

Abstract :

A 3-transistor cell CMOS OTP ROM array using CMOS antifuse (AF) based on permanent breakdown of MOSFET gate oxide is proposed, fabricated and characterized. The proposed 3-T OTP cell for ROM array is composed of an nMOS AF, a high voltage (HV) blocking nMOS, and cell access transistor, all compatible with standard CMOS technology. The experimental results show that the proposed structure can be a viable technology option as a high density OTP ROM array for modern digital as well as analog circuits.