A Wide Range 1.0V-3.6V 200Mbps, Push-Pull Output Buffer Using Parasitic Bipolar Transistors

Takahiro Shimada, Hiromi Notani, Yasunobu Nakase, Hiroshi Makino and Shuhei Iwade System LSI Development Center, Mitsubishi Electric Corporation 4-1 Mizuhara, Itami, Hyogo, 664-8641, Japan E-mail: shimada.takahiro@lsi.melco.co.jp

This paper proposes an output buffer operating from 1.0 V of interface supply voltage VDDX. The driver uses parasitic bipolar transistors to maintain drivability at a lower supply voltage. Furthermore, we introduce a forward body bias control technique in a level converter to avoid speed degradation at a lower internal supply voltage VDD. A test chip was fabricated with a 0.15 μ m CMOS technology, and it achieved 200 Mbps operation at VDDX of 1 V and VDD of 0.7 V.