A Pico-Joule Class, 1 GHz, 32 KByte x 64b DSP SRAM with Self Reverse Bias

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Abstract

New SRAM circuit techniques implemented in a standard, single V_{DD} single V_T 0.13 μm bulk Si CMOS process are reported. These enable pico-joule energy dissipation per accessed bit at 1 GHz and lower total leakage by over 80% from *all* unaccessed cells, during active *and* standby modes, using a self reverse biasing scheme that addresses leakage due to quantum tunneling *and* thermal excitation with an area, performance and noise margin penalty of less than 3%