A CMOS 33-mW 100-MHz 80-dB SFDR Sample-and-Hold Amplifier

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A high-speed high-resolution sample-and-hold amplifier (SHA) is designed for time-interleaved analog-to-digital converter applications. Using the techniques of precharging and output capacitor coupling can mitigate the stringent performance requirements for the opamp, resulting in low power dissipation. Implemented in a standard 0.25 μm CMOS technology, the SHA achieves 80 dB spurious-free dynamic range (SFDR) for a 1.8 Vpp output at 100 MHz Nyquist sampling rate. The SHA dissipates 33 mW from a single 2.5 V supply.