We present circuits for a high-efficiency, low-swing interconnect scheme suitable for a modular, reconfigurable architecture. By using a separate supply, global clocking, and differential signaling, we reduce design complexity; and by using overdrive circuits, equalization techniques, and sense-amplifiers we retain high performance. A testchip built in a 1.8V 0.18-μm technology consumed $<$ 1pJ/bit for a 10mm bus at 1GHz, a power savings over full-swing signaling of up to 10x, and demonstrated amplifier input offset voltages of under 100mV.