The Flexible Processor - Dynamically Reconfigurable Logic Array for Personal-use Emulation System

Takeshi Ohkawa, Toshiyuki Nozawa, Masanori Fujibayashi, Naoto Miyamoto, Karnan Leo, Soichiro Kita, Koji Kotani and Tadahiro Ohmi1

Graduate School of Engineering, Tohoku University ¹New Industry Creation Hatchery Center, Tohoku University 05 Aza Aoba, Aramaki, Aoba-ku, Sendai-shi, Miyagi 980-8579, Japan Phone: +81-22-217-3977 Fax: +81-22-217-3986 E-mail: Ohkawa@fff.niche.tohoku.ac.jp

A dynamically reconfigurable logic array, i.e., the Flexible Processor, suitable for single chip emulation system is developed. It demonstrates the sequential execution of sub-circuits divided from original circuit, by newly developed Temporal Communication Module (TCM). In order to accelerate emulation speed, a logic element, which can reduce configuration data by 30% as compared to conventional Look-Up-Table, is implemented. The chip (3.9x3.9mm²) fabricated with 0.6µm CMOS technology operates at 33MHz with 5.0V power supply.