A 39-to-45-Gbit/s Multi-Data-Rate Clock and Data Recovery Circuit with a Robust Lock Detector

Hideyuki Nosaka, Eiichi Sano*, Kiyoshi Ishii, Minoru Ida, Kenji Kurishima, Shoji Yamahata, and Tsugumichi Shibata

NTT Photonics Laboratories, NTT Corporation
3-1 Morinosato Wakamiya, Atsugi-shi, Kanagawa, 243-0198 Japan
*Now with Research Center for Integrated Quantum Electronics, Hokkaido university

We present a 40-Gbit/s-class clock and data recovery (CDR) circuit with a new lock detector. The CDR IC was fabricated using InP/InGaAs HBTs. Error-free operation and wide eye opening were confirmed for 40, 43, and 45-Gbit/s PRBS with a length of 2^{31} –1. By attaching a frequency search and phase control (FSPC) circuit, the CDR circuit pulls in throughout a 39-45 Gbit/s range. The fabricated IC dissipates 1.89 W at a supply voltage of –4.5V.