## **Experimental Evidence for the Generation of Bulk Traps by Negative Bias Temperature Stress and Their Impact on the Integrity of Direct-tunneling Gate Dielectrics**

Shimpei Tsujikawa, Kikuo Watanabe, Ryuta Tsuchiya, Kazuhiro Ohnishi, and Jiro Yugami Central Research Laboratory, Hitachi, Ltd. 1-280 Higashi-Koigakubo, Kokubunji, Tokyo 185-8601, Japan

NBTI of pMOSFETs with direct-tunneling gate dielectrics was studied. Bulk trap generation in the gate dielectrics during NBT stress was clarified for the first time. We consider that the bulk trap generation is due to hydrogen atoms released from the interface. Moreover, we investigated the impact of the bulk traps on SILC and TDDB, and described strong indications that the same mechanism, namely the hydrogen release, is responsible for both NBTI and TDDB of pMOSFETs.