# Highly Manufacturable Sub-50 nm High Performance CMOSFET Using Real Damascene Gate Process

Chang-Woo Oh, Sung-Ho Kim, Chang-Sub Lee*, Jeong-Dong Choe, Shin-Ae Lee, Sung-Young Lee, Kyung-Hwan Yeo, Hye-Jin Jo, Eun-Jung Yoon, Sang-Jin Hyun**, Donggun Park, and Kinam Kim

ATD, CAE*, and PD** Team, R&D Center, Samsung Electronics Co,
San 24, Nongseo-Ri, Kiheung-Eup, Yongin-City, Kyunggi-Do, KOREA, 449-711
Phone: +82-31-209-6668, Fax: +82-31-209-3274, E-mail: changwoo.oh@samsung.com

We demonstrate highly manufacturable sub-50 nm CMOSFETs using 'real' damascene gate process without dummy gate formation, which has structural merits in scaling resulting from locally implanted channel. The fabricated sub-50nm CMOSFETs show the excellent suppression of short channel effect due to the locally implanted channel and the outstanding current drivability, 810 μA/μm for nMOS and 424 μA/μm for pMOS at $V_{DD}$=1.0 V and $I_{OFF}$ =100 nA/μm. In particular, the pMOS performance is comparable to the state-of-the-art result.