Full Integration and Reliability Evaluation of Phase-change RAM Based on 0.24μm-CMOS Technologies

Y.N. Hwang, J.S. Hong, S.H. Lee, S.J. Ahn, G.T. Jeong, G.H. Koh, J.H. Oh, H.J. Kim, W.C. Jeong, S.Y. Lee, J.H. Park, K.C. Ryoo, H. Horii*, Y.H. Ha*, J.H. Yi*, W.Y. Cho, Y.T. Kim†, K.H. Lee†, S.H. Joo*, S.O. Park*, U.I. Chung*, H.S. Jeong and Kinam Kim
Advanced Technology Development, *Process Development, and †Computer Aided Engineering Teams
Semiconductor R&D Div., Samsung Electronics Co., Ltd
San #24, Nongseo-Ri, Kiheung-Eup, Yongin, Kyunggi-Do 449-900 Korea

We have fully integrated a nonvolatile random access memory by successfully incorporating a reversibly phase-changeable chalcogenide memory element with MOS transistor. As well as basic characteristics of the memory operation, we have also observed reliable performances of the device on hot temperature operation, endurance against repetitive phase transition, writing imprint, reading disturbance and data retention.