Cost-effective Production using Electron Projection Lithography for 65-nm Node SoC and Beyond

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We have established EPL and key infrastructure technology aiming for middle-volume production of SoC and demonstrated fabrication of a 65-nm node ULSI. Overlay accuracy (3σ) for the gate level was less than 30 nm by mix & match and that for the contact level was 20 nm for EPL to EPL. CD uniformity was 6 nm (3σ) . We have also shown its expandability to 45-nm nodes. EPL is promising in cost-effective production of 65-nm and 45-nm nodes less than 3k wafer/mask compared to ArF and F₂.