A novel self-aligned shallow trench isolation cell for 90nm 4Gbit NAND Flash EEPROM s

Masayuki Ichige, Yuji Takeuchi, Kikuko Sugimae, Atsuhiro Sato, Michiharu Matsui, Takeshi Kamigaichi, Hiroyuki Kutsukake, Yutaka Ishibashi, Masanobu Saito, Seiichi Mori***, Hisataka Meguro**, Shoichi Miyazaki**, Tadashi Miwa**, Shinya Takahashi**, Tadashi Iguchi***, Naoto Kawai*, Susumu Tamon*, Norihisa.Arai*, Hideyuki Kamata*, Toshifumi Minami*, Hirohisa Iizuka***, Masaaki Higashitani****, Tuan Pham****, Gertjan Hemink****, Masaki Momodomi* and Riichiro Shirota

SoC R&D Center, Semiconductor Company, Toshiba Corp.,
8 Shinsugita-cho, Isogo-ku, Yokohama city, Japan 235-8211
Phone +81-45-770-3209, FAX +81-45-770-3210, e-mail masayuki.ichige@toshiba.co.jp
*File Memory Device Eng. Gr., Memory Div., Semiconductor Company, Toshiba Corp.,
2-5-1, Kasama, Sakae-ku, Yokohama, Japan 247-8585
** Process & Manufacturing Eng. Center, Semiconductor Company, Toshiba Corp.,
8 Shinsugita-cho, Isogo-ku, Yokohama, Japan 235-8211
** *Advanced Memory Device Gr., Memory Div., Semiconductor Company, Toshiba Corp.,
800,Yamanoisshiki-cho, Yokkaichi, Japan 512-8550
**** SanDisk Corporation,
140 Caspian Court, Sunnyvale, CA, USA 94089-1000

ABSTRACT

Recently, the new memory structures, those FG(floating gate) and AA(active area) are completely self aligned, are qualified for 4Gb NAND flash memory in 90nm technology node. The new cell structure is scalable to sub 90nm node, although the conventional memory cell is hard to scale down to less than 110nm technology node. This paper describes the new structures and these electrical characteristics and also peripheral transistors' performances.