

SESSION 4 – TAPA I DRAM I
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Tuesday, June 15, 1:30 p.m.

Chairpersons: S. Crowder, IBM  
W-S Lee, Samsung Electronics

**4.1 — 1:30 p.m.**

**A 78nm 6F<sup>2</sup> DRAM Technology for Multigigabit Densities**, F. Fishburn, B. Busch, J. Dale, D. Hwang, R. Lane, T. McDaniel, S. Southwick, R. Turi, H. Wang, and L. Tran, Micron Technology, Inc., Boise, ID

This paper discusses a manufacturable 6F<sup>2</sup> DRAM technology at a 78nm half-pitch feature size that results in the smallest DRAM cell size (0.036 $\mu$ m<sup>2</sup>) to date. The novel 6F<sup>2</sup> cell design utilizes line/space patterning and self-aligned etches to improve process margin. An MIM capacitor that employs composite high-k dielectric materials is integrated into the process. Tungsten-clad WL and BL reduce parasitics and noise to make this 6F<sup>2</sup> technology suitable for 2Gb-4Gb density DRAM volume production.

**4.2 — 1:55 p.m.**

**80 nm 512M DRAM with Enhanced Data Retention Time Using Partially-Insulated Cell Array Transistor (PiCAT)**, K.H. Yeo, C.W. Oh, S.-M. Kim, M.-S. Kim, C.-S. Lee, S.-Y. Lee, M. Li, H.-J. Cho, E.-J. Yoon, S.-H. Kim, J.-D. Choe, D.-W. Kim, D. Park and K. Kim, Samsung Electronics Co., Kyungki-Do, Korea

An 80 nm 512M DDR DRAM with partially-insulated cell array transistor (PiCAT) was fabricated. Si/SiGe epitaxial growth and selective SiGe etch process were used to form PiOX (Partially-Insulating OXide) under source and drain of the cell transistor, PiCAT. Using these technologies, partial-SOI (Silicon-On-Insulator) structure could be realized with excellent structural and electrical advantages on bulk Si wafer. Self-limited shallow junction under source/drain and halo doping effect at the channel region were formed by PiOX. With PiCAT, junction leakage current and SCE (Short Channel Effect) were reduced, and excellent data retention time was obtained.

**4.3 — 2:20 p.m.**

**Integrated Device and Process Technology for Sub-70nm Low Power DRAM**, C. Cho, S. Song, S. Kim, S. Jang, S. Lee, H. Kim, J. Park, J. Bae, Y. Ahn, Y. Kim and K. Kim, Samsung Electronics Co., Kyungki-Do, Korea

A novel process technology for 70nm DRAM was for the first time developed. ArFlithography with lithography friendly layout and highly selective etching process were used for patterning of critical layers. A novel gap-fill technology using spin coating oxide was used for STI and ILD processes. Metal tungsten on dual poly gate and dual gate oxide with plasma nitridation process was used for the performance of peripheral transistors. Bar type bit line contact was used to increase the transistor current about 10%. MIM cell capacitor was developed with buried-OCS scheme and 15Å equivalent Tox and 1fA leakage was confirmed.

**4.4 — 2:45 p.m.**

**Novel Robust Cell Capacitor (Leaning Exterminated Ring Type Insulator) and New Storage Node Contact (Top Spacer Contact) for 70nm DRAM Technology and Beyond**, J.M. Park, Y.S. Hwang, D.W. Shin, M. Huh, D.H. Kim, H.K. Hwang, H.J. Oh, J.W. Song, N.J. Kang, B.H. Lee, C.J. Yun, M.S. Shim, S.E. Kim, J.Y. Kim, J.M. Kwon, B.J. Park, J.W. Lee, D.I. Kim, M.H. Cho, M.Y. Jeong, H.J. Kim, H.J. Kim, H.S. Kim, G.Y. Jin, Y.G. Park and K. Kim, Samsung Electronics Co., Kyungki-Do, Korea

For the first time, novel robust capacitor (Leaning exterminated Ring type Insulator - LERI) and new storage node (SN) contact process (Top Spacer Contact- TSC) are successfully developed with 82nm feature size. These novel processes drastically improved electrical characteristics such as cell capacitance, parasitic bit line capacitance and cell contact resistance, compared to a conventional process. The most pronounced effect using the LERI in COB structure is to greatly improve cell capacitance without twin bit failure. In addition, the TSC technology has an ability to remove a critical ArF lithography. By using the LERI and TSC processes in 82nm 512M DDR DRAM, the cell capacitance of 32fF/cell is achieved with Toxeq of 2.3nm and the parasitic bit line capacitance is reduced by 20%, resulted in great improvement of tRCD(1.5ns).