SESSION 16 – TAPA II
Nyquist ADC 1

Friday, June 16, 1:30 p.m.
Chairpersons: K. Nakamura, Analog Devices
H. Yamazaki, Fujitsu Laboratories Ltd.

16.1 – 1:30 p.m.
A 6-bit 800-MS/s Pipelined A/D Converter with Open-loop Amplifiers, D.-L. Shen, T.-C. Lee, National Taiwan University, Taipei, Taiwan

A 6-bit 800-MS/s pipelined A/D converter (ADC) with voltage-mode open-loop amplifiers achieves SNDR and SFDR of 33.7 dB and 47.5 dB, respectively. Fabricated in a 0.18-µm CMOS technology, the ADC consumes 105 mW from a 1.8-V power supply while the active area is only 0.5-mm^2.

16.2 – 1:55 p.m.
A 1-V 100MS/s 8-bit CMOS Switched-Opamp Pipelined ADC Using Loading-Free Architecture, Y. Wu, V.S.L. Cheung, H. Luong, Hong Kong University of Science and Technology, Kowloon, Hong Kong

A 1V, 8-bit dual-mode ADC is realized using multi-phase switched-opamp (SO) technique. Employing a proposed load-ing-free pipelined ADC architecture and a fast-wake-up dual-input-dual-output switchable opamp, the ADC achieves 100MS/s conversion rate, which is the fastest operation speed reported at 1-V supply, and comparable to many high-voltage switched-capacitor (SC) ADC. Implemented in a 0.18µm CMOS process, the ADC obtains a peak SNR of 45dB and SFDR of 52.6dB while dissipating only 30mW.

16.3 – 2:20 p.m.
A 7bit 800Msps 120mW Folding and Interpolation ADC Using a Mixed-Averaging Scheme, K. Makigawa, K. Ono, T. Ohkawa, K. Matsuura, M. Segami, Sony Corp., Kanagawa, Japan

A 7bit 800Msps folding and interpolation ADC is presented. This ADC uses new offset-averaging schemes in preamplifiers and current-mode interpolation stages and a digital-averaging scheme in a comparator stage to operate at higher speed with low power dissipation. The measured SNR is 36.8dB at a 200MHz input frequency. The prototype of the complete ADC is fabricated in a 90nm digital CMOS process and consumes 120mW with 2.5V and 1.2V supply.

16.4 – 2:45 p.m.
A 500MS/s 5b ADC in 65nm CMOS, B.P. Ginsburg, A.P. Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA

A 1.2V 6mW 500MS/s 5-bit ADC for use in a UWB receiver has been fabricated in a pure digital 65nm CMOS technology. The ADC uses a 6-channel time-interleaved successive approximation register architecture. Each of the channels has a split capacitor array to reduce switching energy and sensitivity to digital timing skew. A variable delay line is used to optimize the instant of latch strobing to reduce preamplifier currents.