SESSION 2 – TAPA II
SRAM Cell Stability

Thursday, June 15, 10:00 a.m.
Chairpersons: A. Amerasekera, Texas Instruments
T. Kawahara, Hitachi

2.1 – 10:00 a.m.
Wordline & Bitline Pulsing Schemes for Improving SRAM Cell Stability in Low-Vcc 65nm CMOS Designs, M. Khellah, Y. Ye, N.S. Kim, D. Somasekhar, G. Pandya, A. Farhang, K. Zhang, C. Webb, V. De, Intel, Hillsboro, OR

Pulsed Wordline (PWL) & Pulsed Bitline (PBL)techniques to improve SRAM cell stabilities in single-Vcc microprocessor designs are evaluated in 65nm CMOS. At 0.7V Vcc, PWL improves cell failure rate by 15X while incurring <1% area overhead. Both PBL & PWL with Read-Modify-Write (PWL-RMW) provide the best improvements (26X) in cell stability, with significant area overheads (4-8%).

2.2 – 10:25 a.m.
A Stable SRAM Cell Design Against Simultaneously R/W Disturbed Accesses, T. Suzuki, H. Yamauchi*, Y. Yamagami, K. Satomi, H. Akamatsu, Matsushita Electric Industrial Co., Ltd., Kyoto, Japan, *Fukuoka Institute of Technology, Fukuoka, Japan

The cell-margin against a simultaneously read and write disturbed accesses even in the same column is required to a 2-port SRAM. We have developed the new cell design for an 8-Tr 2-port cell in a 65-nm CMOS and the R/W margins were improved by 45%/70%, respectively at 0.9V, and the cell-size reduced by 20% compared with the conventional column-based Vdd control. Another 7-Tr cell which reduced cell-area by 31% is also demonstrated.

2.3 – 10:50 a.m.
A Vth-Variation-Tolerant SRAM with 0.3-V Minimum Operation Voltage for Memory-Rich SoC under DVS Environment, Y. Morita, H. Fujiwara*, H. Noguchi*, K. Kawakami*, J. Miyakoshi*, S. Mikami, K. Nii*, H. Kawaguchi*, M. Yoshimoto*, Kanazawa University, *Kobe University, Kobe, Japan

This paper proposes a voltage-control scheme for an SRAM that makes a minimum operation voltage down to 0.3 V even on a future memory-rich SoC. A self-aligned timing control guarantees stable operation in a wide range of Vdd under DVS environment. A measurement result of a 64-kb SRAM in a 90-nm process technology shows that 30% power reduction is achieved at 100 MHz. The area overhead is only 5.6%.

2.4 – 11:15 a.m.
An SRAM Design in 65nm and 45nm Technology Nodes Featuring Read and Write-Assist Circuits to Expand Operating Voltage, H. Pilo, J. Barwin, G. Braceras, C. Browning, S. Burns, J. Gabric, S. Lamphier, M. Miller, A. Roberts, F. Towler, IBM Systems and Technology Group, Essex Junction, VT

This paper describes a 32Mb SRAM that has been designed and fabricated in a 65nm low-power CMOS Technology. The design has also been migrated to 45nm Bulk and SOI technologies. The 68mm2 die features read and write-assist circuit techniques that expand the operating voltage range and improve manufacturability across technology platforms. Hardware results show improved failure rates when assist features are invoked.

2.5 – 11:40 a.m.
A 65 nm SoC Embedded 6T-SRAM Design for Manufacturing with Read and Write Cell Stabilizing Circuits, S. Ohbayashi, M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Imaoka*, Y. Oda*, M. Igarashi, M. Takeuchi, H. Kawashima, H. Makino, Y. Yamaguchi, K. Tsukamoto, M. Inuishi, K. Ishibashi, H. Shinohara, Renesas Technology Corp., Hyogo, Japan, *Renesas Design Corp., Hyogo, Japan

We propose a new design scheme to improve the SRAM read and write operation margins in the presence of a large Vth variability. By applying this scheme to a 0.494 μm^2 SRAM cell with a β ratio of 1, which is an aggressively small cell size, we can achieve a high-yield 8M-SRAM for a wide range of Vth value using a 65 nm LSTP CMOS technology.