SESSION 21 – TAPA I
Advanced Memory and Circuits

Saturday, June 17, 8:30 a.m.
Chairpersons: S. Natarajan, Emerging Memory Technologies, Inc.
K. Kajigaya, Elpida Memory, Inc.

**21.1 – 8:30 a.m.**
**A 128Mb Floating Body RAM(FBRAM) on SOI with Multi-Averaging Scheme of Dummy Cell,** T. Ohsawa, T. Higashi*, K. Fujita, K. Hatsuda, N. Ikumi, T. Shino, H. Nakajima, Y. Minami, N. Kusunoki, A. Sakamoto**, J. Nishimura, T. Hamamoto, S. Fujii, Toshiba Corp., *Toshiba Microelectronics Corp., **Toshiba Information Systems Corp., Yokohama, Japan

A 128Mb FBRAM using the floating body cell (FBC) or the 1T DRAM cell the size of 0.17um$^2$(6.24F2 with F=0.165um)was successfully fabricated and tested. The multi-averaging method of dummy cell was shown to be effective in increasing the bit yield of the RAM to 99.999%, making the chip fixable by redundancy. The write method we employed was shown to make the RAM free of any BL disturb. The WL disturb caused by the charge pumping was also avoided by an implemented restore circuit.

**21.2 – 8:55 a.m.**
**A Configurable Enhanced T$^2$RAM Macro for System Level Power Management Unified Memory,** K. Arimoto, F. Morishita, I. Hayashi, T. Gyohten, H. Noda, T. Ipposhi, K. Dosaka, Renesas Technology Corp., Hyogo, Japan

TTRAM can provide the high speed/low power and high density with CMOS compatible SOI process. However it is difficult to handle as the unified memory required for advanced SoC because it needs the simple control sensing operation for memory compiler, higher cell efficiency, and lower voltage operation for dynamic frequency and voltage control. The enhanced TTRAM (ET$^2$RAM) can solve these issues and the key technologies provide 0.5V memory operation, compact and higher sensitivity sense amplifier, and programmable multi-bank array.

**21.3 – 9:20 a.m.**
**A 3-Transistor DRAM Cell with Gated Diode for Enhanced Speed and Retention Time,** W.K. Luk, J. Cai, R.H. Dennard, M.J. Immediato, S.V. Kosonocky, IBM T.J. Watson Research Center, Yorktown Heights, NY

3T1D is a non-destructive read DRAM cell with three transistors (T) and a gated diode (D). The gated diode acts as a storage device and an amplifier, leading to low voltage, high speed and high tolerance to variability, and comparing favorably to conventional 3T gain cell and 6T SRAM cell. Hardware measurements in 90 nm SOI showed the 3T1D achieved longer retention than the 3T. Retention, speed and scaling perspectives for future technology are presented.

**21.4 – 9:45 a.m.**
**Low Power SOC Design Using Partial-Trench-Isolation ABC SOI (PTI-ABC SOI) for Sub-100-nm LSTP Technology,** O. Ozawa, K. Fukuoka, Y. Igarashi, T. Kuraishi, Y. Yasu, Y. Maki, T. Ipposhi, T. Ochiai, M. Shirahata, K. Ishibashi, Renesas Technology Corp., Tokyo, Japan

The bodies of partially depleted SOI devices are selectively biased so that circuits operate at low supply voltages without area overhead. Applying forward body bias to logic gates reduces delay variation by 7-21%. A level shifter (LF) and Data-Retention-FF (DRFF) circuits can operate at lower supply voltages below 1.0-V when the body bias of the key transistors is suitably controlled. The technology reduces operating and standby power of SOC with 90-nm LSTP CMOS technology by 40 and 98%, respectively.

**21.5 – 10:10 a.m.**
**A Register File with 8.4GHz Throughput for Efficient Instruction Scheduling in a Pentium® 4 Processor,** N. Nintunze, G. Pham, Intel Corp., Hillsboro, OR

This paper describes a unique register file(RF) for ping-pong operation in 65nm CMOS process. The merged ping-pong reduces array width by 50%, doubles the frequency of access, and allows for same phase read and write. Implementation as a dependency matrix allows for all read wordlines to be asserted at once. A bypass scheme merged with the bitline contributes to a 27% leakage saving.