SESSION 25 – TAPA II
Nyquist ADCs II

Saturday, June 17, 10:50 a.m.
Chairpersons: K. Gulati, BitWave Semiconductor
M. Nagata, Kobe University

25.1 – 10:50 a.m.
A 15b-Linear, 20MS/s, 1.5b/Stage Pipelined ADC Digitally Calibrated with Signal-Dependent Dithering, Y.-S. Shu, B.-S. Song, University of California, San Diego, CA

A signal-dependent dithering concept is developed to measure the multiplying DAC (MDAC) gain error of a 1.5b/stage pipelined ADC in background. A 15b, 20MS/s prototype ADC exhibits SFDR and THD of 98 and -92dB with 14.5MHz input. The chip fabricated in 0.18 micron CMOS occupies 2.3mm x 1.7mm, and consumes 285mW at 1.8V.

25.2 – 11:15 a.m.
A 12b 10MS/s Pipelined ADC Using Reference Scaling, G. Ahn, P.K. Hanumolu, M. Kim, S. Takeuchi*, T. Sugimoto*, K. Hamashita*, K. Takasuka*, G. Temes, U. Moon, Oregon State University, Corvallis, OR, *Asahi Kasei Microsystems, Atsugi, Japan

A 12b 10MS/s pipelined ADC using reference scaling achieves 62 dB SNDR and 72 dB SFDR for a 1MHz input. The prototype IC fabricated in a 0.35um CMOS process employs interstage amplifiers with 45dB open-loop gain and consumes 19mW from a 2.4V supply.

25.3 – 11:40 a.m.
A 12b, 75MS/s Pipelined ADC Using Incomplete Settling, E. Iroaga, B. Murmann, Stanford University, Stanford, CA

This paper proposes a mixed-signal technique that exploits incomplete settling to achieve ultra low power residue amplification. In the first stage of the presented 12-bit, 75-MS/s prototype ADC, the employed open-loop gain stage dissipates only 2.9mW from a 3V supply, achieving a 94% power reduction over a typical op-amp implementation. The complete pipelined ADC achieves a measured SNR of 66dB (fin=1MHz), consumes 273mW and occupies 7.9mm^2 in 0.35mm CMOS.

25.4 – 12:05 p.m.
A 1V 30mW 10b 100MSample/s Pipeline A/D Converter Using Capacitance Coupling Techniques, K. Honda, F. Masanori, S. Kawahito, Shizuoka University, Hamammatsu, Japan

A 10b 100MSample/s pipeline A/D converter in 90nm process consumes 30mW at 1.0V power supply. The proposed capacitance coupling S/H stage and capacitance coupled class-AB amplifier achieve low distortion and low power dissipation at high-speed sampling. The SNDR and SFDR at 100MHz sampling are 54.0 dB and 70.0 dB, respectively.

25.5 – 12:30 p.m.
A 10b 170MS/s CMOS Pipelined ADC Featuring 84dB SFDR without Calibration, J. Li, G. Manganaro, M. Courcy, B.-M. Min, L. Tomasi*, A. Alam*, R. Taylor*, National Semiconductor, Salem, NH, *National Semiconductor, Phoenix, AZ

A 0.85mm^2 3.3V 10b 170MS/s CMOS pipelined ADC using opamp-sharing technique in a 0.35um/0.18um CMOS process is presented. The overhead of the opamp-sharing scheme is significantly reduced using 0.18um-long devices as sampling switches and local regulators providing the switch drivers' supply. With a 10MHz input signal, the ADC achieves 83.8dB SFDR and 9.36ENOB at 171MS/s. Better than 9.26ENOB are maintained for inputs up to 100MHz consuming 180mW at 3.3V.