SESSION 26 – TAPA III
RF Front Ends and
Baseband Processing

Saturday, June 17, 10:50 a.m.
Chairpersons: A. Abidi, University of California, Los Angeles
M. Ito, Renesas Technology

26.1 – 10:50 a.m.
A 0.5 V 900 MHz CMOS Receiver Front End, N. Stanic, P. Kinget, Y. Tsividis, Columbia University, New York, NY

A 900 MHz RF receiver front end including an LNA, downconversion mixer and associated LO buffers is presented. All circuits operate from a 0.5 V supply without any internal voltage boosting. The circuit is designed in 0.18 um standard CMOS. It achieves a conversion gain of 12 dB, an IIP3 of -14 dBm and a noise figure of 9 dB. The circuit, including the LO buffers, dissipates 7.4 mW and occupies an active area of 0.43 mm^2.

26.2 – 11:15 a.m.
Multi-band (1-6GHz), Sampled, Sliding-IF Receiver With Discrete-Time-Filtering in 90nm Digital CMOS Process, H. Lakdawala, J. Zhan, A. Ravi, S. Anderson, B.R. Carlton, R.B. Nicholls, N. Yaghini, R.E. Bishop, S.S. Taylor, K. Soumyanath, Intel Corp., Hillsboro, OR

A prototype 1-6GHz multi-band sampled sliding-IF receiver with discrete-time channel select filtering in a 90nm low resistivity substrate, strained-Si digital CMOS process is presented. The core receiver has an inductor-less wideband LNA front-end, a sampled mixer, and a combination of programmable poly-phase FIR and IIR filter for baseband filtering. The receiver achieves a Noise Figure (NF) of <13.5dB and IIP3 of >-19dBm for bands between 1-6GHz. The receiver when used in a system with an external tuned LNA (2.5dB NF) on the front end module achieves NF of <7dB, and IIP3 of >-34dBm for the WiFi bands. The die area for the entire receiver is 0.9mm2 and consumes 89mW.

26.3 – 11:40 a.m.
A Cartesian-Feedback Linearized CMOS RF Transmitter for EDGE Modulation, L. Tee, E. Sacchi*, R. Bocock, N. Wongkomet, P.R. Gray, University of California, Berkeley, CA, *STMicroelectronics, Pavia, Italy

A 1.55GHz CMOS RF transmitter with an integrated Class-C Power Amplifier (PA) is described. The transmitter uses Cartesian Feedback to meet EDGE linearity requirements and integrates a direct-conversion modulator, PA, LO phase shifter, feedback mixers and baseband loop filter in a 0.18µm CMOS process. The transmitter produces an 18dBm EDGE modulated output with 18% drain efficiency. Keywords: CMOS, EDGE, Cartesian feedback, linearization and transmitter.

26.4 – 12:05 p.m.
A 1V 14mW-per-Channel Flexible-IF CMOS Analog-Baseband IC for 802.11a/b/g Receivers, P.-I. Mak, S.-P. U*, R.P. Martins**, University of Macau, Macao, China, *Chipidea Microelectronics, Ltd., Macao, China, **Instituto Superior Tecnico, Lisbon, Portugal

Presented is a low-voltage low-power analog-baseband IC featuring a two-step channel-selection architecture for a flexible-IF reception of 802.11a/b/g. In circuits, it integrates innovatively series-switching mixers for a precise I/Q demodulation; an inside-OpAmp dc-offset cancellation for area savings and switchability, a switched-current-resistor programmable-gain amplifier for a transient-free constant-bandwidth gain adjustment. Fabricated in a 0.35um CMOS process, each channel consumes 14mW from 1V, while measuring <1µs gain-switched transient, 32/90dB stopband rejection at 20/40MHz and 15.2dBm IIP3.

26.5 – 12:30 p.m.
A 31.2mW UWB Baseband Transceiver with All-Digital I/Q-mismatch Calibration and Dynamic Sampling, J.-Y. Yu, C.-C. Chung, H.-Y. Liu, Y.-W. Lin, W.-C. Liao, T.-Y. Hsu, C.-Y. Lee, National Chiao-Tung University, Taiwan

A MB-OFDM UWB baseband transceiver with I/Q-mismatch (IQM) calibration and dynamic sampling (DS) is presented. It calibrates IQM by 2dB gain and 20 degree phase errors, releasing IQM tolerance to 10x of existing designs. The DS reduces ADC sampling rate to 1/9 ~ 1/2 of existing designs, resulting in at least 43% ADC power saving. Measured power consumes 31.2mW at 480Mb/s data rate