SESSION 4 – IOLANI I-IV
Clock Generation for High Speed Transceivers

Thursday, June 15, 10:00 a.m.
Chairpersons: G. Taylor, Intel Corp.
M. Mizuno, NEC Corp.

4.1 – 10:00 a.m.
A 1.2V 37-38.5GHz 8-Phase Clock Generator in 0.13um CMOS Technology, C. Lee, L.-C. Chou, S.-I. Liu, C.-L. Ko*, Y.-Z. Juang*, C.-F. Chiu*, National Taiwan University, Taipei, Taiwan, *National Applied Research Lab, Hsinchu, Taiwan

A 37-38.5GHz octave-phase clock generator is presented. An octave-phase LC voltage-controlled oscillator and the split-load divider are presented. The proposed PD improves the static phase error and enhances the gain. The clock generator has been fabricated in 0.13um CMOS technology. It achieves the rms jitter of 0.24ps at 38GHz while consuming 51.6mW without buffers from a 1.2V supply.

4.2 – 10:25 a.m.
A Low-Jitter PLL and Repeaterless Clock Distribution Network for a 20Gb/s Link, F. O'Mahony, M. Mansuri, B. Casper, J.E. Jaussi, R. Mooney, Intel Corp., Hillsboro, OR

A 10GHz clock generation and distribution network for an 8-channel 20Gb/s/channel data transmitter is demonstrated in a 90nm 1.2V CMOS process. Jitter due to power supply and device noise is minimized with an LC VCO and repeaterless clock network. The performance of the forwarded-clock link degrades by only 4% due to ±5% supply noise at the transmitter. The LC VCO achieves supply noise sensitivity of 200MHz/V (0.02%-frequency/1%-supply noise) and short-term (8-symbol) rms jitter of 100fs. The clock distribution network delay sensitivity to supply noise is 36ps/V. The total clocking power is 408mW.

4.3 – 10:50 a.m.
A Digital PLL with a Stochastic Time-to-Digital Converter, V. Kratyuk, P.K. Hanumolu, K. Ok, K. Mayaram, U.-K. Moon, Oregon State University, Corvallis, OR

A new dual-loop digital PLL (DPLL) architecture is presented. It employs a stochastic time-to-digital converter (STDC) and a high frequency delta-sigma dithering to achieve a wide PLL bandwidth and low jitter at the same time. The test chip has been fabricated in a 0.13um CMOS process. The DPLL features a 0.7-1.7GHz oscillator tuning range, 6.9ps rms jitter and consumes 17mW while operating at 1.2GHz.

4.4 – 11:15 a.m.
An Ultra-Wide Range Digitally Adaptive Control Phase Locked Loop with New 3-Phase Switched Capacitor Loop Filter, S. Dosho, N. Yanagisawa, K. Sogawa, Y. Yamada, T. Morie, Matsushita Electric Industrial Co. Ltd., Osaka, Japan

This paper describes an ultra-wide range adaptive-biased Phase Locked Loop. In order to tolerate the wide variation of the input frequency, the capacitance of the filter and the VCO gain are optimized digitally in addition to the charge pump current. The new switched capacitor filter which realizes the fully flat response was developed to make the filter as small as possible. Measured period jitter(=12sigma) is below 1.55 % of the output clock period.

4.5 – 11:40 a.m.
A Multiphase Delay-Locked Loop for 0.125-2Gbps 0.18µm CMOS Transmitter, Y. Moon, D. Shim, Silicon Image Inc., Sunnyvale, CA

A 0.18-um CMOS DLL generates equally-spaced multiphase clocks over 16x range from 31.25 to 500MHz using a duty-cycle corrector and a lock detector with 32x lock range, which is at least 3.5x wider comparing with conventional multiphase DLLs. Measured TX data eyes have <4% eye unevenness, which is equivalent to <1% clock unevenness, over the data rates of 0.125 to 2Gbps.