SESSION 5 – TAPA II
RF Blocks for Tuners and Sensor Networks

Thursday, June 15, 1:30 p.m.
Chairpersons: F. Dai, Auburn University
K. Agawa, Toshiba Corp.

5.1 – 1:30 p.m.
A Fully-Integrated 0.13µm CMOS Low-IF DBS Satellite Tuner, A. Maxim, R. Poorfard, R. Johnson, P. Crawley, J. Kao, Z. Dong, M. Chennam, T. Nutt, D. Trager, Silicon Laboratories Inc., Austin, TX

The first low-IF fully-integrated tuner for DBS satellite TV applications was realized in 0.13 µm CMOS. A wide bandwidth, ring oscillator integer-N frequency synthesizer having a large frequency step was used to down-convert a cluster of channels to a coarsely defined low-IF frequency, while the second down-conversion to base-band was performed in the digital domain. Eliminating the oscillator inductors has reduced the parasitic magnetic coupling from the digital circuitry, allowing a single-chip integration of the sensitive tuner and the noisy demodulator, while bringing a significant die area reduction.

5.2 – 1:55 p.m.
A 184mW Fully Integrated DVB-H Tuner Chip with Distortion Compensated Variable Gain LNA, H. Kawamura, T. Fujiwara, K. Kagoshima, S. Kawama, H. Kijima, M. Koutani, S. Toyoyama, K. Sakuno, K. Iizuka, Sharp Corp., Nara, Japan

A single chip direct conversion DVB-H tuner with a distortion compensated variable gain LNA is implemented in 0.5um SiGe BiCMOS. The LNA exhibits 0dBm IIP3 and 2.8dB NF at 860MHz. A new offset cancel feedback is introduced that keeps the cutoff frequency independent of the baseband gain. The IC consumes 184mW at 2.8V while achieving a sensitivity of -96dBm for QPSK, CR=1/2 signal.

5.3 – 2:20 p.m.
9.75/10.6GHz SiGe PLL for LNB Satellite Front-Ends Using Half-Rate Oscillators, A. Maxim, M. Gheorghe, C. Turinici, Integrated Products, Austin, TX

A fully-integrated frequency synthesizer for DBS satellite front-ends was realized in a low cost 50GHz fT SiGe process. Two half-rate VCOs followed by Gilbert frequency doublers generate the 9.75/10.6 GHz LO signals with lower phase noise than a full-rate oscillator. The loop filter was integrated on-chip by using a passive feed-forward architecture, which provides a noiseless resistor multiplication.

5.4 – 2:45 p.m.
A 46% Efficient 0.8dBm Transmitter for Wireless Sensor Networks, Y.H. Chee, A.M. Niknejad, J. Rabaey, University of California, Berkeley, CA

This paper presents a 1.9GHz low power transmitter for wireless sensor networks. It uses Film Bulk Acoustic Resonators (FBAR) for RF carrier generation and is co-designed with the antenna. The two-channel transmitter is 46% efficient when radiating 1.2mW from a 650mV supply. With 50% on-off keying, it consumes 1.35mW and supports data rate up till 330kbps. The $1.2x0.8mm^2$ transmitter is implemented in 0.13um CMOS and is integrated into a $38x25x8.5mm^3$ solar powered sensor node.