2006 VLSI Technology Short Course
TAPA I/II

Process Technologies for Continued Scaling and Performance

Monday, June 12, 2006, 9:00 a.m.

Organizers: Robert Chau, Intel Corporation
Toshihiro Sugii, Fujitsu Laboratories, Ltd.

9:00 a.m. **Back-end Interconnect Technology**
C.H. Jan, Intel Corp.

10:00 a.m. **Break**

10:15 a.m. **Advanced Embedded Memories**
K. Ishimaru, Toshiba Corp.

11:15 a.m. **Lithography Solutions for 32nm and Beyond**
M. Kameyama, Nikon Corp.

12:15 p.m. **Lunch**

2:00 p.m. **Ultra-Shallow Junction Technologies**
M. Kase, Fujitsu, Ltd.

3:00 p.m. **Device Technology**
S. Thompson, University of Florida

4:00 p.m. **Break**

4:15 p.m. **High-k Gate Dielectrics**
J. Lee, University of Texas at Austin

5:15 p.m. **Conclusion**

Welcome to the 2006 Symposium on VLSI Technology!

On behalf of the organizing Committees, it is our pleasure to invite you to attend the 2006 Symposium on VLSI Technology which will be held from June 13-15 in Honolulu, Hawaii.

Since its founding in 1982, this symposium has been one of the most prestigious international forums for the latest research and development in VLSI technology. The program committee has worked very hard this year to select 92 excellent contributed papers from 296 submissions and organized them into 23 sessions. We are also delighted to have two distinguished Invited Speakers for the Plenary Session. Dr. Hans Stork of Texas Instruments, will speak on “Balancing SoC Design and Technology Challenges at 45nm” and Professor Hiroshi Ishiguro of Osaka University will present a talk on” Interactive Humanoids and Androids”.

In addition, Professor Sugano will be honored during the opening session for his many years of insightful leadership since the beginning of the conference.

The conference will also have three Rump Sessions on the evening of June 14 as a means to facilitate informal discussions among researchers. One is a joint session with the Symposium on VLSI Circuits which will address "Power Management- how will it be solved for 32nm and beyond?" The other two sessions will cover specific technology related topics of current interest;

- 3D Integration
- Embedded Memories in the 21st Century

In addition, there will be a one-day Short Course on Monday June 12 and will cover "Process Technologies for Continued Scaling and Performance”. Six distinguished researchers will discuss various aspects of deeply scaled CMOS technology. The Short Course promises to be an excellent opportunity for experienced as well as new engineers to broaden their technical base.

The symposium registration fee covers all of the sessions including the Rump Sessions, coffee breaks, Monday night Reception and the Tuesday night Banquet. Registration for the Short Course is extra. The registration fees and hotel reservation schedules are detailed at the end of the Advance Program.

As in past years, we expect a strong participation of top VLSI researchers from both the industry and the academic sectors. We look forward to seeing you at this year’s exciting Symposium in Honolulu.

Jason Woo	Tohru Mogami
Program Chair	Program Co-Chair

SESSION I – TAPA I
Plenary Session

Tuesday, June 13, 8:00 a.m. – 10:00 a.m.
Chairpersons: Jason Woo, University of California
Tohru Mogami, NEC Corp.

8:15 a.m. **Welcome and Opening Remarks**
Bob Havemann, Novellus Systems, Inc.
Shin'ichiro Kimura, Hitachi, Ltd.

1.1 – 8:30 a.m.
Balancing SoC Design and Technology Challenges at 45nm
Hans Stork, Texas Instruments

1.2 – 9:15 a.m.
Interactive Humanoids and Androids
Hiroshi Ishguro, Osaka University

10:00 a.m. **Break**

SESSION 2 – TAPA I
Advanced High K Metal Gate Stacks Integration

Tuesday, June 13, 10:15 a.m.
Chairpersons: S. Biesemans, IMEC
M. Niwa, Matsushita Electric Industrial Co., Ltd.

2.1 – 10:15 a.m.
Thermally Stable N-Metal Gate MOSFETs Using La-Incorporated HfSiO Dielectric, H.N. Alshareef, H.R. Harris, H.C. Wen, C.S. Park, C. Huffmann, K. Choi, H.F. Luan, P. Majhi, B.H. Lee, R. Jammy, D.J. Lichtenwalner*, J.S. Jur*, A.I. Kingon*, SEMATECH, Austin, TX, *North Carolina State University, Raleigh, NC

2.2 – 10:40 a.m.
Dual Metal Gates with Band-Edge Work Functions on Novel HfLaO High- *κ* Gate Dielectric, X.P. Wang[1,2], C. Shen[1,2], M.-F. Li[1,2], H.Y. Yu[3], Y. Sun[1], Y.P. Feng[1], A. Lim[1], H.W. Sik[1], A. Chin[4], Y.C. Yeo[1], P. Lo[2], D. L. Kwong[2], [1]National University of Singapore, Singapore, [2]Institute of Microelectronics, Singapore, [3]IMEC, Leuven, Belgium, [4]National Chiao-Tung University, Hsinchu, Taiwan

2.3 – 11:05 a.m.
Advanced Dual Metal Gate MOSFETs with High-*k* Dielectric for CMOS Application, P.F. Hsu, Y.T. Hou, F.Y. Yen, V.S. Chang, P.S. Lim, C.L. Hung, L.G. Yao, J.C. Jiang, H.J. Lin, J.M. Chiou, K.M. Yin, J.J. Lee, R.L. Hwang, Y. Jin, S.M. Chang, H.J. Tao, S.C. Chen, M.S. Liang, T.P. Ma*, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, *Yale University, New Haven, CT

2.4 – 11:30 a.m.
Highly Manufacturable 45nm LSTP CMOSFETs Using Novel Dual High-k and Dual Metal Gate CMOS Integration, S.C. Song, Z.B. Zhang, M.M. Hussain, C. Huffman, J. Barnett, S.H. Bae, H.J. Li, P. Majhi, C.S. Park, B.S. Ju, H.K. Park, C.Y. Kang*, R. Choi, P. Zeitzoff, H.H. Tseng, B.H. Lee, R. Jammy, SEMATECH, Austin, TX, *GIST, Korea

11:55 a.m. **Lunch**

SESSION 3 – TAPA II
Advanced Flash Memory

Tuesday, June 13, 10:15 a.m.
Chairpersons: L. Tran, Micron Technology
S.S. Chung, National Chiao-Tung University

3.1 – 10:15 a.m.
A 60nm NOR Flash Memory Cell Technology Utilizing Back Bias Assisted Band-to-Band Tunneling Induced Hot-Electron Injection (B4-Flash), S. Shukuri, N. Ajika, M. Mihara, K. Kobayashi, T. Endoh*, M. Nakashima, GENUSION, Inc., Hyogo, Japan, *Tohoku University, Sendai, Japan

3.2 – 10:40 a.m.
Fully 3-Dimensional NOR Flash Cell with Recessed Channel and Cylindrical Floating Gate – A Scaling Direction for 65nm and Beyond, S.-P. Sim, K.S. Kim, H.K. Lee, J.I. Han, W.H. Kwon, J.H. Han, B.Y. Lee, C. Jung, J.H. Park, D.J. Kim, D.H. Jang, W.H. Lee, C. Park. K. Kim, Samsung Electronics Co. Ltd., Gyeonggi-Do, Korea

3.3 – 11:05 a.m.
A 64-Cell NAND Flash Memory with Asymmetric S/D Structure for Sub-40nm Technology and Beyond, K.-T. Park, J. Choi, J. Sel, V. Kim, C. Kang, Y. Shin, U. Roh, J. Park, J.-S. Lee, J. Sim, S. Jeon, C. Lee, K. Kim, Samsung Electronics Co. Ltd., Kyungki-Do, Korea

3.4 – 11:30 a.m.
Multi-Level NAND Flash Memory with 63 nm-node TANOS (Si-Oxide-SiN-Al_2O_3-TaN) Cell Structure, C.-H. Lee, J. Choi, C. Kang, Y. Shin, J.-S. Lee, J. Sel, J. Sim, S. Jeon, B.-I. Choe, D. Bae, K. Park, K. Kim, Samsung Electronics Co. Ltd., Kyungki-Do, Korea

11:55 a.m. Lunch

SESSION 4 – TAPA I
Advanced Gate Dielectric Reliability

Tuesday, June 13, 1:30 p.m.
Chairpersons: A. Lacaita, Politecnico di Milano
Y. Omura, Kansai University

4.1 – 1:30 p.m.
A Comparative Study of NBTI and PBTI (Charge Trapping) in SiO_2/HfO_2 Stacks with FUSI, TiN, Re Gates, S. Zafar, Y.H. Kim, V. Narayanan, C. Cabral Jr., V. Paruchuri, B. Doris, J. Stathis, A. Callegari, M. Chudzik, IBM Semiconductor Research & Development Center, Yorktown Heights, NY

4.2 – 1:55 p.m.
Impact of Crystalline Phase of Ni-FUSI Gate Electrode on BTI and TDDB Reliability of HfSiON MOSFETs, M. Terai, T. Onizawa, S. Kotsuji, A. Toda, S. Fujieda, H. Watanabe, NEC Corp., Sagamihara, Japan

4.3 – 2:20 p.m.
Impact of Polarity and Hf Concentration on Breakdown of HfSiON/SiO_2 Gate Dielectrics, M. Sato, I. Hirano, T. Aoyama, K. Sekine, T. Kobayashi, T. Yamaguchi, K. Eguchi, Y. Tsunashima, Toshiba Corporation, Yokohama, Japan

4.4 – 2:45 p.m.
Newly Found Anomalous Gate Leakage Current (AGLC) for 65 nm Node and Beyond, and Its Countermeasure Using Nitrogen Implanted Poly-Si, M. Togo, T. Suzuki, E. Hasegawa, S. Koyama, T. Fukai, A. Sakakidani, S. Miyake, T. Watanabe, I. Yamamoto, M. Tanaka*, Y. Kawashima, Y. Kunimune, M. Ikeda, K. Imai, NEC Electronics Corp., Kanagawa, Japan, *NEC Corp., Kanagawa, Japan

3:10 p.m. Break

SESSION 5 – TAPA II
Advanced Dynamic Memory

Tuesday, June 13, 1:30 p.m.
Chairpersons: L. Tran, Micron Technology
R. Yamada, Hitachi, Ltd.

5.1 – 1:30 p.m.
Highly Scalable Saddle-Fin(S-Fin) Transistor for Sub-50nm DRAM Technology, S.-W. Chung, S.-D. Lee, S.-A. Jang, M.-S. Yoo, K.-O. Kim, C.-O. Chung, S.Y. Cho, H.-J. Cho, L.-H. Lee, S.-H. Hwang, J.-S. Kim, B.-H. Lee, H.G. Yoon, H.-S. Park, S.-J. Baek, Y.-S. Cho, N.-J. Kwak, H.-C. Sohn, S.-C. Moon, K.-D. Yoo, J.-G. Jeong, J.-W. Kim, S.-J. Hong, S.-W. Park, Hynix Semiconductor Inc., Kyoungki-Do, Korea

5.2 – 1:55 p.m.
A Full FinFET DRAM Core Integration Technology Using a Simple Selective Fin Formation Technique, M. Yoshida, J. Kahng, C. Lee, S.-M. Jang, H. Sung, K. Kim, H.-J. Kim, K.-H. Jung, W. Yang, D. Park, B.-I. Ryu, Samsung Electronics Co., Kyunggi-Do, Korea

5.3 – 2:20 p.m.
Vertex Channel Field Effect Transistor (VC-FET) Technology Featuring High Performance and Highly Manufacturable Trench Capacitor DRAM, M. Kido, M. Kito, R. Katsumata, M. Kondo, S. Ito, K. Matsuo*, K. Miyano*, I. Mizushima*, M. Sato, H. Tanaka, H. Yasutake, Y. Nagata**, T. Hoshino^, N. Aoki, H. Aochi, A. Nitayama, Toshiba Corporation , Semiconductor Company, Kanagawa, Japan, * SoC Research & Development Center and Process & Manufacturing Engineering Center, Kanagawa, Japan, **Toshiba Information Systems Corporation, Kanagawa, Japan, ^Toshiba Microelectronics Corporation, Kanagawa, Japan

5.4 – 2:45 p.m.
Development of New TiN/ZrO_2/Al_2O_3/ZrO_2/TiN Capacitors Extendable to 45nm Generation DRAMs Replacing HfO_2 based Dielectrics, D.-S. Kil, H.-S. Song, K.-J. Lee, K. Hong, J.-H. Kim, K.-S. Park, S.-J. Yeom, J.-S. Roh, N.-J. Kwak, H.-C. Sohn, J.-W. Kim, S.-W. Park, Hynix Semiconductor Inc., Kyoungki-Do, Korea

3:10 p.m. Break

SESSION 6 – TAPA I
Non-Volatile Trapped Charge Memory

Tuesday, June 13, 3:25 p.m.
Chairpersons: K.-M. Chang, Freescale
J.H. Lee, MagnaChip Semiconductor Inc.

6.1 – 3:25 p.m.
A 4-Bit Double SONOS Memory (DSM) with 4 storage Nodes per Cell for Ultimate Multi-Bit Operation, C.W. Oh, S.H. Kim, N.Y. Kim, Y.L. Choi, K.H. Lee, B.S. Kim, N.M. Cho, S.B. Kim, D.-W. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Kyungki-Do, Korea

6.2 – 3:50 p.m.
A Novel Non-Volatile Memory Cell Using a Gated-Diode Structure with a Trapping-Nitride Storage Layer, W.J. Tsai, T.F. Ou, H.L. Kao, E.K. Lai, Y.Y. Liao, C.C. Yeh, T. Wang, J. Ku, C.-Y. Lu, Macronix International Co. Ltd., Hsin-Chu, Taiwan

6.3 – 4:15 p.m.
Very Low Voltage SiO_2/HfON/HfAlO/TaN Memory with Fast Speed and Good Retention, C.H. Lai, A. Chin, H.L. Kao, K.M. Chen, M. Hong*, J. Kwo*, C.C. Chi*, National Chiao-Tung University, Hsinchu, Taiwan, *National Tsing Hua University, Hsinchu, Taiwan

6.4 – 4:40 p.m.
A Highly Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory, E.-K. Lai, H.-T. Lue, Y.-H. Hsiao, J.-Y. Hsieh, S.-C. Lee, C.-P. Lu, S.-Y. Wang, L.-W. Yang, K.-C. Chen, J. Gong*, K.-Y. Hsieh, J. Ku, R. Liu, C.-Y. Lu, Macronix International Co. Ltd., Hsinchu, Taiwan, *National Tsing Hua University, Hsinchu, Taiwan

6.5 – 5:05 p.m.
A Novel Multi-Functional Silicon-On-ONO (SOONO) MOSFETs for SoC Applications : Electrical Characterization for High Performance Transistor and Embedded Memory Applications, C.W. Oh, S.H. Kim, N.Y. Kim, Y.L. Choi, Y.S. Lee, W.J. Jang, H.S. Lee, H.S. Park, D.-W. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Kyungki-Do, Korea

SESSION 7 – TAPA II
Multi-Gate FETs

Tuesday, June 13, 3:25 p.m.
Chairpersons: T.-J. King Liu, Synopsys, Inc.
M. Masahara, AIST

7.1 – 3:25 p.m.
Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering, J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, R. Chau, Intel Corporation, Hillsboro, OR

7.2 – 3:50 p.m.
Performance Enhancement of MUGFET Devices Using Super Critical Strained–SOI (SC-SSOI)and CESL, N. Collaert, R. Rooyackers, F. Clemente, P. Zimmerman, I. Cayrefourcq*, B. Ghyselen*, K.T. San^, B. Eyckens, M. Jurczak, S. Biesemans, IMEC, Leuven, Belgium, *SOITEC, Crolles Cedex, France, ^Texas Instruments Inc., Dallas, TX

7.3 – 4:15 p.m.
Investigation of FinFET Devices for 32nm Technologies and Beyond, H. Shang, L. Chang, X. Wang, M. Rooks, Y. Zhang, B. To, K. Babich, G. Totir, Y. Sun, E. Kiewra, M. Ieong, W. Haensch, IBM Semiconductor Research and Development Center, Yorktown Heights, NY

7.4 – 4:40 p.m.
Strained N-Channel FinFETs with 25 nm Gate Length and Silicon-Carbon Source/Drain Regions for Performance Enhancement, T.-Y. Liow[1,2], K.-M. Tan[1], R. T. P. Lee[1], A. Du[2], C.-H. Tung[2], G. S. Samudra[1], W.-J. Yoo[1], N. Balasubramanian[2], Y.-C. Yeo[1], [1]National University of Singapore, Singapore, [2]Institute of Microelectronics, Singapore

7.5 – 5:05 p.m.
Sub-5nm All-Around Gate FinFET for Ultimate Scaling, H. Lee, L.-E. Yu, S.-W. Ryu, J.-W. Han, K. Jeon, D.-Y. Jang, K.-H. Kim, J. Lee, J.-H. Kim, S.C. Jeon*, G.S. Lee*, J.S. Oh*, Y.C. Park*, W.H. Bae*, H.M. Lee*, J.M. Yang*, J.J. Yoo*, S.I. Kim*, Y.-K. Choi, Korea Advanced Institute of Science and Technology, Daejeon, Korea, *Korean National Nanofab Center, Daejeon, Korea

SESSION 8 – TAPA I
Strain Enhanced CMOS I

Wednesday, June 14, 8:30 a.m.
Chairpersons: T. Grider, Texas Instruments
T. Hiramoto, University of Tokyo

8.1 – 8:30 a.m.
Stress Proximity Technique for Performance Improvement with Dual Stress Liner at 45nm Technology and Beyond, X. Chen, S. Fang, W. Gao[1], T. Dyer, Y. W. Teh[1], S. S. Tan[1], Y. Ko[3], C. Baiocco, A. Ajmera, J. Park[3], J. Kim[3], R. Stierstorfer[2], D. Chidambarrao, Z. Luo, N. Nivo, P. Nguyen, J. Yuan, S. Panda, O. Kwon[2], N. Edleman, T. Tjoa[1], J. Widodo[1], M. Belyansky, M. Sherony, R. Amos, H. Ng, M. Hierlemann[2], D. Coolbough, A. Steegen, I. Yang, J. Sudijono[1], T. Schiml[2], J. H. Ku[3], C. Davis, IBM Semiconductor Research and Development Center, Hopewell Junction, NY, [1]Chartered Semiconductor Manufacturing, [2]Infineon Technologies AG, [3]Samsung Electronics Co. Ltd.

8.2 – 8:55 a.m.
1-D and 2-D Geometry Effects in Uniaxially-Strained Dual Etch Stop Layer Stressor Integrations, P. Grudowski, V. Adams, X.-Z. Bo, K. Loiko, S. Filipiak, J. Hackenberg, M. Jahanbani, M. Azrak, S. Goktepeli, M. Shroff, W.-J. Liang*, S.J. Lian*, V. Kolagunta, N. Cave, C.-H. Wu*, M. Foisy, H.C. Tuan*, J. Cheek, Freescale Semiconductor Inc., Austin, TX, *Taiwan Semiconductor Manufacturing Company

8.3 – 9:20 a.m.
Scalable eSiGe S/D Technology with Less Layout Dependence for 45-nm Generation, K. Ota, T. Sanuki*, K. Yahashi*, Y. Miyanami, K. Matsuo*, J. Idebuchi*, M. Moriya, K. Nakayama*, R. Yamaguchi*, H. Tanaka*, T. Yamazaki, S. Terauchi, A. Horiuchi, S. Fujita, I. Mizushima*, H. Yamasaki*, K. Nagaoka, A. Oishi*, Y. Takegawa*, K. Ohno, M. Iwai*, M. Saito, F. Matsuoka*, N. Nagashima, Sony Corporation, Kanagawa, Japan, *Toshiba Corporation, Kanagawa, Japan

8.4 – 9:45 a.m.
50 nm Silicon-On-Insulator N-MOSFET Featuring Multiple Stressors: Silicon-Carbon Source/Drain Regions and Tensile Stress Silicon Nitride Liner, K.-W. Ang, K.-J. Chui, H.-C. Chin, Y.-L. Foo^, A. Du*, W. Deng*, M.-F. Li, G. Samudra, N. Balasubramanian*, Y.-C. Yeo, National University of Singapore, Singapore, *Institute of Microelectronics, Singapore, ^Institute of Materials Research & Engineering, Singapore

10:10 a.m. Break

SESSION 9 – TAPA II
High Speed Memory Technology

Wednesday, June 14, 8:30 a.m.
Chairpersons: C. Dennison, Ovonyx Technologies, Inc.
H. Oyamatsu, Toshiba

9.1 – 8:30 a.m.
122 Mb High Speed SRAM Cell with 25nm Gate Length Multi-Bridge-Channel MOSFET (MBCFET) on Bulk Si Substrate, M.S. Kim, S.-Y. Lee, E.-J. Yoon, S.M. Kim, J. Lian, K.-H. Lee, N.M. Cho, M.-S. Lee, D. Hwang, Y.-S. Lee, D.-W. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Kyoungi-Do, Korea

9.2 – 8:55 a.m.
Embedded Bulk FinFET SRAM Cell Technology with Planar FET Peripheral Circuit for *hp*32 nm Node and Beyond, H. Kawasaki, K. Okano, A. Kaneko, A. Yagishita, T. Izumida, T. Kanemura, K. Kasai, T. Ishida, T. Sasaki, Y. Takeyama, N. Aoki, N. Ohtsuka, K. Suguro, K. Eguchi, Y. Tsunashima, S. Inaba, K. Ishimaru, H. Ishiuchi, Toshiba Corporation Semiconductor Company, Yokohama, Japan

9.3 – 9:20 a.m.
TiN/HfSiO$_x$ Gate Stack Multi-Channel Field Effect Transistor (McFET) for sub 55nm SRAM Application, S.M. Kim, E.J. Yoon, M.S. Kim, S.D. Suk, M. Li, L. Jun, C.W. Oh, K.H. Yeo, S.H. Kim, S.Y. Lee, Y.L. Choi, N.-Y. Kim, Y.-Y. Yeoh, H.-B. Park, C.S. Kim, H.-M. Kim, D.-C. Kim, H.S. Park, H.D. Kim, Y.M. Lee, D.-W. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Kyoungi-Do, Korea

9.4 – 9:45 a.m.
Highly Reliable and Scalable Tungsten Polymetal Gate Process for Memory Devices Using Low-Temperature Plasma Selective Gate Reoxidation, K.-Y. Lim, M.-G. Sung, H.-J. Cho, Y.S. Kim, S.-A. Jang, J.-G. Oh, S.R. Lee, K. Kim, P.-S. Lee, Y.-S. Chun, H.-S. Yang, N.-J. Kwak, H.-C. Sohn, J.-W. Kim, S.-W. Park, Hynix Semiconductor Inc., Kyoungki-Do, Korea

10:10 a.m. Break

SESSION 10 – TAPA I
Mobility Enhancement on Process Induced Strain

Wednesday, June 14, 10:25 a.m.
Chairpersons: F. Nouri, Applied Materials Inc.
T. Kuroi, Renesas Technology Corp.

10.1 – 10:25 a.m.
Integration of Local Stress Techniques with Strained-Si Directly On Insulator (SSDOI) Substrates, H. Yin, Z. Ren, H. Chen, J. Holt, X. Liu*, J. W. Sleight, K. Rim, V. Chan, D.M. Fried, Y.H. Kim*, J.O. Chu*, B.J. Greene, S.W. Bedell*, G. Pfeiffer, R. Bendernagel, D.K. Sadana*, T. Kanarsky, C.Y. Sung*, M. Ieong*, G. Shahidi*, IBM Semiconductor Research and Development Center, Hopewell Junction, NY, *IBM T.J. Watson Research Center, Yorktown Heights, NY

10.2 – 10:50 a.m.
Stress Memorization Technique (SMT) Optimization for 45nm CMOS, C. Ortolland[1,5], P. Morin[2], C. Chaton[3], E. Mastromatteo[1], C. Populaire[4], S. Orain[1], F. Leverd[2], P. Stolk[1], F. Boeuf[2], F. Arnaud[2], [1]Philips Semiconductors, Crolles, France, [2]STMicroelectronics, Crolles, France, [3]CEA-LETI, Crolles, France, [4]Freescale Semiconductor, Crolles, France, [5]Laboratoire Physique de la Matiere, Villeurbanne, France

10.3 – 11:15 a.m.
NiSi Schottky Barrier Process-Strained Si (SB-PSS) CMOS Technology for High Performance Applications, C.H. Ko, H.W. Chen, T.J. Wang, T.M. Kuan, J.W. Hsu, C.Y. Huang, C.H. Ge, L.S. Lai, W.C. Lee, Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan

10.4 – 11:40 a.m.
A Low Cost Drive Current Enhancement Technique Using Shallow Trench Isolation Induced Stress for 45-nm Node, C. Le Cam, F. Guyader*, C. de Buttet**, P. Guyader*, G. Ribes*, M. Sardo*, S. Vanbergue, F. Boeuf*, F. Arnaud*, E. Josse*, M. Haond*, Philips Semi., Crolles, France, *STMicroelectronics, Crolles, France, **Freescale Semi., Crolles, France

12:05 p.m. Lunch

SESSION 11 – TAPA II
Non-Volatile FinFet Flash Memory

Wednesday, June 14, 10:25 a.m.
Chairpersons: T.-J. King Liu, Synopsys, Inc.
J. T. Moon, Samsung Electronics Co., Ltd.

11.1 – 10:25 a.m.
Paired FinFET Charge Trap Flash Memory for Vertical High Density Storage, S. Kim, W. Kim, J. Hyun, S. Byun, J. Koo, J. Lee, K. Cho, S. Lim, J. Park, I.-K. Yoo, C.-H. Lee*, D. Park*, Y. Park, Samsung Advanced Institute of Technology, Gyeonggi-Do, Korea, *Samsung Elec. Co., Gyeonggi-Do, Korea

11.2 – 10:50 a.m.
SONOS-type FinFET Device Using P^+ Poly-Si Gate and High-k Blocking Dielectric Integrated on Cell Array and GSL/SSL for Multi-Gigabit NAND Flash Memory, S.-K. Sung, S.-H. Lee, B.Y. Choi, J.J. Lee, J.-D. Choe, E.S. Cho, Y.J. Ahn, D. Choi, C.-H. Lee, D.H. Kim, Y.-S. Lee, S.B. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Gyeonggi-Do, Korea

11.3 – 11:15 a.m.
Trap Layer Engineered FinFET NAND Flash with Enhanced Memory Window, Y.J. Ahn, J.-D. Choe, J.J. Lee, D. Choi, E.S. Cho, B.Y. Choi, S.-H. Lee, S.-K. Sung, C.-H. Lee, S.H. Cheong, D.K. Lee, S.B. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Gyeonggi-Do, Korea

11.4 – 11:40 a.m.
Technology Breakthrough of Body-Tied FinFET for Sub 50 nm NOR Flash Memory, E.S. Cho T.-Y. Kim, B.K. Cho, C.-H. Lee, J.J. Lee, A. Fayrushin, C. Lee, D. Park, B.-I. Ryu, Samsung Electronics Co., Gyeonggi-Do, Korea

12:05 p.m. Lunch

SESSION – 12
Advanced FUSI Gates Stacks

Wednesday, June 14, 1:30 p.m.
Chairpersons: T. Skotnicki, STMicroelectronics
K. Shibahara, Hiroshima University

12.1 – 1:30 p.m.
Novel FUSI Strained Engineering for 45-nm Node CMOS Performance Enhancement, C.T. Lin, C.H. Hsu, L.W. Chen, T.F. Chen, C.R. Hsu, C.H. Lin, S. Chiang, D.C. Cho, C.T. Tsai, G.H. Ma, United Microelectronics Corporation, Hsin-Chu City, Taiwan

12.2 – 1:55 p.m.
Dual Work Function Phase Controlled Ni-FUSI CMOS (NiSi NMOS, Ni_2Si or $Ni_{31}Si_{12}$ PMOS): Manufacturability, Reliability & Process Window Improvement by Sacrificial SiGe Cap, A. Veloso, T. Hoffman, A. Lauwers, S. Brus, J.-F. de Marneffe, S. Locorotondo, C. Vrancken, T. Kauerauf, A. Shickova, B. Sijmus, H. Tigelaar, M.A. Pawlak, H.Y. Yu, C. Demeurisse, S. Kubicek, C. Kerner, T. Chiarella, O. Richard, H. Bender, M. Niwa, P. Absil, M. Jurczak, S. Biesemans, J.A. Kittl, IMEC, Leuven, Belgium

12.3 – 2:20 p.m.
Suppression Effects of Threshold Voltage Variation with Ni FUSI Gate Electrode for 45nm Node and Beyond LSTP and SRAM Devices, Y. Okayama, T. Saito, K. Nakajima, S. Taniguchi, T. Ono, K. Nakayama, R. Watanabe, A. Oishi, A. Eiho, T. Komoda, T. Kimura, M. Hamaguchi, Y. Takegawa, T. Aoyama, T. Iinuma, K. Fukasaku*, R. Morimoto*, K. Oshima*, K. Oono*, M. Saito*, M. Iwai, S. Yamada, N. Nagashima*, F. Matsuoka, Toshiba Corporation, Yokohama, Japan, *Sony Corporation, Yokohama, Japan

12.4 – 2:45 p.m.
Demonstration of a New Approach Towards 0.25V Low-Vt CMOS Using Ni-based FUSI, H.Y. Yu, J.A. Kittl, A. Lauwers, R. Singanamalla, C. Demeurisse, S. Kubicek, E. Augendre, A. Veloso, S. Brus, C. Vrancken, T. Hoffman, S. Mertens, B. Onsia, R. Verbeeck, M. Demand, A. Rothchild, B. Froment, M. van Dal, K. De Meyer, M.F. Li*, J.D. Chen*, M. Jurczak, P.P. Absil, S. Biesemans, IMEC, Leuven Belgium, *National University of Singapore, Singapore

3:10 p.m. Break

SESSION 13 – TAPA II
Analog/RF/Mixed-Signal VLSI

Wednesday, June 14, 1:30 p.m.
Chairpersons: C. Bulucea, National Semiconductor Corp.
T. Dan, Sanyo Electric Co., Ltd.

13.1 – 1:30 p.m.
A 45nm Low Cost Low Power Platform by Using Integrated Dual-Stress-Liner Technology, J. Yuan, S.S. Tan[1], Y.M. Lee[1], J. Kim[2], R. Lindsay[3], V. Sardesai, T. Hook, R. Amos, Z. Luo, W. Lee[1], S. Fang, T. Dyer, N. Rovedo, R. Stierstorfer[3], Z. Yang, J. Li, K. Barton, H. Ng, J. Sudijono[1], J. Ku[2], M. Heirlemann[3], T. Schiml[3], IBM Semiconductor Research and Development Center, Hopewell Junction, NY, [1]Chartered Semiconductor Manufacturing Limited, [2]Samsung Electronics Co. Ltd., [3]Infineon Technologies AG

13.2 – 1:55 p.m.
High Performance Micro-Crystallized TaN/$SrTiO_3$/TaN Capacitors for Analog and RF Applications, K.C. Chiang, C.C. Huang, A. Chin, W.J. Chen*, H.L. Kao, M. Hong**, J. Kwo**, National Chiao-Tung University, Hsinchu, Taiwan, *National Ping-Tung University of Science and Technology, Taiwan, **National Tsing Hau University, Hsinchu, Taiwan

13.3 – 2:20 p.m.
Improved 1/f Noise Characteristics in Locally Strained Si CMOS using Hydrogen-Controlled Stress Liners and Embedded SiGe, T. Ueno, H.S. Rhee, H. Lee, M.S. Kim, H.S. Cho*, H.S. Baik*, Y.H. Jung, H.W. Lee, H.S. Park, C.K. Lee, G.-J. Bae, N.-I. Lee, Samsung Electronics Co. Ltd., Kyunggi-Do, Korea, *SAIT, Kyunggi-Do, Korea

13.4 – 2:45 p.m.
Impact of HfSiON Induced Flicker Noise on Scaling of Future Mixed-Signal CMOS, Y. Yasuda[1,2], C.-H. Lin[1], T.-J. King Liu[1], C. Hu[1], [1]University of California, Berkeley, California, [2]NEC Electronics Corporation

3:10 p.m. Break

SESSION 14 – TAPA I
Advanced Interconnect Technology

Wednesday, June 14, 3:25 p.m.
Chairpersons: B. van Schravendijk, Novellus Systems, Inc.
Y. Takao, Fujitsu Ltd.

14.1 – 3:25 p.m.
High-performance Cu-interconnects with Novel Seamless Low-k SiOCH Stacks (SEALS) Featured by Compositional Modulation Process for 45nm-node ULSI Devices, M. Tagami, H. Ohtake, M. Tada, M. Ueki, F. Ito, T. Taiji*, Y. Kasama*, T. Iwamoto, H. Wakabayashi, T. Fukai*, K. Arai, S. Saito, H. Yamamoto, M. Abe, M. Narihiro, N. Furutake, T. Onodera, T. Takeuchi, Y. Tsuchiya*, N. Oda*, M. Sekine*, M. Hane, Y. Hayashi, NEC Corporation, Kanagawa, Japan, *NEC Electronics Corporation, Kanagawa, Japan

14.2 – 3:50 p.m.
Thermally and Chemically Robust, Non-Reflowable Low-*k* Spin-on Glass (*k* = 2.4) for Gap-filling Technology in Sub-50-nm Memory Devices, D. Ryuzaki, H. Sakurai, T. Yoshikawa, K. Torii, Hitachi Chemical Co. Ltd., Tokyo, Japan

14.3 – 4:15 p.m.
Direct Non-contact Electrical Measurement of Low-k Damage in Patterned Low-k Films by a Near-Field Scanned Microwave Probe, J.S. Tsai, J.W. Hsu, V.V. Talanov*, A. Scherz*, A.R. Schwartz*, J.H. Shieh, S.M. Jang, M.S. Liang, Taiwan Semiconductor Manufacturing Co. Ltd., Hsinchu, Taiwan, *Neocera, Inc., Beltsville, MD

14.4 – 4:40 p.m.
Integration of Self-Formed Barrier Technology for 32nm-node Cu Dual-Damascene Interconnects with Hybrid Low-k (PAr/SiOC) Structure, Y. Ohoka, K. Inoue, T. Hayashi, N. Komai, S. Arakawa, R. Kanamura, S. Kadomura, Sony Corporation, Kanagawa, Japan

14.5 – 5:05 p.m.
Lower Resistance Scaled Metal Contacts to Silicide for Advanced CMOS, A. Topol, C. Sheraw*, K. Wong*, X. Shao, R. Knarr*, S. Rossnagel, C.-C. Yang*, B. Baker-O'Neal, A. Simon*, B. Haran, Y. Li*, C. Ouyang, S. Allen*, C. Brodsky*, S. Cohen, L. Deligianni, X. Chen*, S. Deshpande*, C.Y. Sung*, M. Ieong, IBM T. J. Watson Research Center, Yortown Heights, NY, *IBM Systems and Technology, Hopewell Junction, NY

SESSION 15 – TAPA II
Alternative Non-Volatile Memory

Wednesday, June 14, 3:25 p.m.
Chairpersons: C. Dennison, Ovonyx Technologies, Inc.
T. Nakamura, Rohm Co., Ltd.

15.1 – 3:25 p.m.
Highly Reliable 256Mb PRAM with Advanced Ring Contact Technology and Novel Encapsulating Technology, Y.J. Song, K.C. Ryoo, Y.N. Hwang, C.W. Jeong, D.W. Lim, S.S. Park, J.I. Kim, J.H. Kim, S.Y. Lee, J.H. Kong, S.J. Ahn, S.H. Lee, J.H. Park, J.H. Oh, Y.T. Oh, J.S. Kim, J.M. Shin, J.H. Park, Y. Fai, G.H. Koh, G.T. Jeong. R.H. Kim, H.S. Lim, I.S. Park, H.S. Jeong, K. Kim, Samsung Electronics Co. Ltd., Kyunggi-Do, Korea

15.2 – 3:50 p.m.
Novel One-Mask Self-Heating Pillar Phase Change Memory, T.D. Happ*, M. Breitwisch, A. Schrott, J.B. Philipp*, M.H. Lee**, R. Cheek, T. Nirschl*, M. Lamorey, C.H. Ho**, S.H. Chen**, C.F. Chen**, E. Joseph, S. Zaidi*, G.W. Burr, B. Yee, Y.C. Chen**, S. Raoux, H.L. Lung**, R. Bergmann*, C. Lam, IBM, Yorktown Heights, NY, *Infineon Technologies, **Macronix International Co. Ltd.

15.3 – 4:15 p.m.
A 90nm Phase Change Memory Technology for Stand-Alone Non-Volatile Memory Applications, F. Pellizzer, A. Benvenuti, B. Gleixner*, Y. Kim*, B. Johnson*, M. Magistretti, T. Marangon, A. Pirovano, R. Bez, G. Atwood*, STMicroelectronics, Agrate Brianza, Italy, *Intel Corporation, Santa Clara, CA

15.4 – 4:40 p.m.
World Smallest 0.34μm^2 COB Cell 1T1C 64Mb FRAM with New Sensing Architecture and Highly Reliable MOCVD PZT Integration Technology, Y.M. Kang, H.J. Joo, J.H. Park, S.K. Kang, J.-H. Kim, S.G. Oh, H.S. Kim, J.Y. Kang, J.Y. Jung, D.Y. Choi, E.S. Lee, S. Y. Lee, H.S. Jeong, K. Kim, Samsung Electronics Co. Ltd., Kyungki-Do, Korea

15.5 – 5:05 p.m.
High Density and High Reliability Chain FeRAM with Damage-Robust MOCVD-PZT Capacitor with $SrRuO_3/IrO_2$ Top Electrode for 64Mb and Beyond, O. Hidaka, T. Ozaki, H. Kanaya, Y. Kumura, Y. Shimojo, S. Shuto, Y. Yamada, K. Yahashi, K. Yamakawa, S. Yamazaki, D. Takashima, T. Miyakawa, S. Shiratake, S. Ohtsuki*, I. Kunishima, A. Nitayama, Toshiba Corporation, Yokohama, Japan, *Toshiba Microelectronics Corporation, Yokohama, Japan

TECHNOLOGY RUMP SESSIONS
Wednesday, June 14
8:00 p.m. – 10:00 p.m.

Organizers: Shahin Sharifzadeh, Cypress Semi.
Renichi Yamada, Hitachi, Ltd.

RJ1 Power Management: What are the Device and Circuit Trade-offs. How Will it be Managed at 45nm and 32nm Nodes

Tapa I
Organizers:

Circuits	**Technology**
K. Nowka, IBM	H. Puchner, Cypress
Y. Oowaki, Toshiba	T. Ipposhi, Renesas

Moderator: T. Skotnicki, STMicroelectronics

Power management has historically focused on low standby and operating power for mobile devices to increase the battery time. In today's designs, it is increasingly important to optimize power for all electronic applications. Data centers can consume the power of small cities. Previous efforts for power reduction have been focusing on technology as well as design options to reduce standby power. However, it is not clear which of the options will be available in future designs and what other limitations will arise from these reduction techniques. The discussion panel is a compilation of design and process experts and will present views on power management for the 45-nm and 32-nm technology nodes. The panelists will present classical power reduction techniques such as gate leakage, sleeper transistors, cascading, fundamental improvements in leakage performance due to new device architectures. Various techniques will be debated on their merits for high-power vs low-power products or memory-intensive vs logic-dominated designs and technologies.

Panelists

Y. Urakawa, Toshiba	R. Kumar, Intel Corp
U. Ko, Texas Instruments	Y. Yamagata, NEC Electronics
D. Frank, IBM	D. Ditzel, Transmeta

R2: Embedded Memory in the Early 21st Century

Honolulu I
Moderator: S. Thompson, University of Florida
A. Nitayama, Toshiba

Two trends are making embedded memories a winning strategy: slowing of technology scaling and product requirements for large memories. A panel of industry experts will discuss

(1) Application field /market segmentations and forecast in next 10 years: consumer products, portable communication products, high-end products

(2) Forecast of dominant technologies. What e-memory technology will dominate the SoC memory markets during next 10 years?

(3) Volatile vs. Non-volatile or unified memory? When will unified memory be realized?

Panelists:

T. Ning, IBM
K. Zhang, Intel
C. Wang, TSMC
S. Fujii, Toshiba
K.-M. Chang, Freescale

R2: 3-D Integration

Honolulu II

Moderators: K. Saraswat, Stanford University
M. Koyanagi. Tohoku University

The unprecedented growth of the computer and the information technology industry is demanding ULSI circuits with increasing functionality and performance at minimum cost and power dissipation. ULSI circuits are being aggressively scaled to meet this demand. This in turn has introduced some very serious problems for the semiconductor industry. Scaling is reducing gate delays but rapidly increasing interconnect delays. Increasing drive for the integration of disparate signals and technologies is introducing various system-on-a-chip (SoC) design concepts, for which existing planar (2-D) IC design may not be suitable. 3-D chip design strategy that exploits the vertical dimension could alleviate the interconnect related problems and could facilitate SoC applications through heterogeneous integration. However there are many questions to be resolved. For which products 3D makes sense? There are many promising technologies, (wafer bonding, layer transfer, crystallization, epitaxial growth) for manufacturing 3-D ICs. Which technology is useful for which system application? Is 3D technology viable economically? One of the major concerns in 3-D ICs arises due to increased power. Will we have advanced heat sinking technology necessary to achieve maximum performance from the 3D chips?

Panelists:

C. Keast, Massachusetts Institute of Technology
S. Wong, Stanford University
R. Madurawe, VICICIV
A. Matsuzawa, Tokyo Institute of Technology
K. Takahashi, Toshiba
K. Lee, Samsung

SESSION 16 – TAPA I
Strain Enhanced CMOS II

Thursday, June 15, 8:30 a.m.

Chairpersons: F. Nouri, Applied Materials Inc.
H. Matsuhashi, OKI Electric Industry Co., Ltd.

16.1 – 8:30 a.m.

Strain Controlled CMOSFET with Phase Controlled Full-Silicide (PC-FUSI)/HfSiON Gate Stack Structure for 45nm-node LSTP Devices, M. Saitoh, T. Ogura, K. Takahashi, T. Hase, A. Toda, N. Ikarashi, M. Oshida, T. Tatsumi, H. Watanabe, NEC Corporation, Kanagawa, Japan

16.2 – 8:55 a.m.
Strain-Enhanced CMOS Through Novel Process-Substrate Stress Hybridization of Super-Critically Thick Strained Silicon Directly on Insulator (SC-SSOI), A.V-Y. Thean, D. Zhang, V. Vartanian, V. Adams, J. Conner, M. Canonico, H. Desjardin, P. Grudowski, B. Gu, Z.-H. Shi, S. Murphy, G. Spencer, S. Filipiak, D. Goedeke, X.-D. Wang, B. Goolsby, V. Dhandapani, L. Prabhu, S. Backer, L.-B. La, D. Burnett, T. White, B.-Y. Nguyen, B.E. White, S. Venkatesan, J. Mogab, I. Cayrefourcq*, C. Mazure*, Freescale Semiconductor Inc., Austin, TX, *SOITEC, Crolles Cedex, France

16.3 – 9:20 a.m.
Silicon-on-Insulator MOSFETs with Hybrid Crystal Orientations, M. Yang, K. Chan, A. Kumar, S.-H. Lo, J. Sleight, L. Chang, R. Rao, S. Bedell, A. Ray, J. Ott, J. Patel, C. D'Emic, J. Rubino, Y. Zhang, L. Shi, S. Steen, E. Sikorski, J. Newbury, R. Meyer, B. To, P. Kozlowski, W. Graham, S. Maurer, S. Medd, D. Canaperi, L. Deligianni, J. Tornello, G. Gibson, T. Dalton, M. Ieong, G. Shahidi, IBM Semiconductor Research and Development Center, Yorktown Heights, NY

16.4 – 9:45 a.m.
25nm Short and Narrow Strained FDSOI with TiN/HfO_2 Gate Stack, F. Andrieu, C. Dupre, F. Rochette, O. Faynot, L. Tosti, C. Buj, E. Rouchouze*, M. Casse, B. Ghyselen**, I. Cayrefourcq**, L. Brevard, F. Allain, J.C. Barbe, J. Cluzel, A. Vandooren[#], S. Denorme*, T. Ernst, C. Fenouillet-Beranger, C. Jahan, D. Lafond, H. Dansas, B. Previtali, J.P. Colonna, H. Grampeix, P. Gaud, C. Mazure**, S. Deleonibus, CEA/LETI, Grenoble, France, *STMicroelectronics, Crolles Cedex, France, [#]Freescale Semiconductor, Crolles Cedex, France, **SOITEC, Bernin, France

10:10 Break

SESSION 17 – HONOLULU SUITE
Novel Architectures and Process Integration

Thursday, June 15, 8:30 a.m.
Chairpersons: M. Ieong, IBM TJ Watson Research Ctr.
N. Nagashima, Sony Corp.

17.1 – 8:30 a.m.
Pre-Metal Dielectric Stress Engineering by a Novel Plasma Treatment and Integration Scheme for nMOS Performance Improvement, Y.-K. Jeong, D.S. Shin, A. Kim, I.Y. Yoon, S.-W. Nam, S.-J. Lee, K.-K. Park, K.C. Kim, H.-J. Shin, K.B. Roh, K.-H. Kang, Y.-H. Choi, G.-H. Seo, K. Lee, K.S. Chu, N.-I. Lee, Samsung Electronics Co. Ltd., Kyungki-Do, Korea

17.2 – 8:55 a.m.
A Novel Cu Electrical Fuse Structure and Blowing Scheme Utilizing Crack-Assisted Mode for 90-45nm-Node and Beyond, T. Ueda, H. Takaoka, M. Hamada, Y. Kobayashi, A. Ono, NEC Electronics Corporation, Kanagawa, Japan

17.3 – 9:20 a.m.
A New Route to Ultra-High Density Memory Using the Micro to Nano Addressing Block (MNAB), R.S. Shenoy, K. Gopalakrishnan, C. T. Rettner, L.D. Bozano, R.S. King, B. Kurdi, H.K. Wickramasinghe, IBM Almaden Research Center, San Jose, California

17.4 – 9:45 a.m.
The Features and Characteristics of 5-mega CMOS Image Sensor with Topologically Unique 1.7µm x 1.7µm pixels, S.-H. Lee, C.-R. Moon, K.-H. Paik, S.-H. Hwang, J.-C. Shin, J. Jung, K. Lee, H. Noh, D. Lee, K. Kim, Samsung Electronics Co., Gyeonggi-Do, Korea

10:10 Break

SESSION 18 – TAPA I
Strain Enhanced High
Performance PMOS Devices

Thursday, June 15, 10:25 p.m.
Chairpersons: T. Grider, Texas Instruments
M. Masahara, AIST

18.1 – 10:25 a.m.
Strained-Si, Relaxed-Ge Or Strained-(Si)Ge For Future Nanoscale p-MOSFETs?, T. Krishnamohan, D. Kim, C. Jungemann*, Y. Nishi, K.C. Saraswat, Stanford University, Stanford, CA, *Technical University of Braunschweig, Germany

18.2 – 10:50 a.m.
Relationship Between Hole Mobility and Current Drive Enhancement in Uniaxially Strained Thin-Body SiGe-on-Insulator pMOSFETs, T. Tezuka, T. Irisawa, T. Numata, Y. Moriyama, N. Hirashita, E. Toyoda*, K. Usuda, N. Sugiyama, S.-I. Takagi**, MIRAI-ASET, Kawasaki, Japan, *Toshiba Ceramics, Kawasaki, Japan, **MIRAI-AIST, Kawasaki, Japan

18.3 – 11:15 a.m.
Superior Current Enhancement in SiGe Channel p-MOSFETs Fabricated on (110) Surface, P.W. Liu, J.W. Pan, T.Y. Chang, T.L. Tsai, T.F. Chen, Y.C. Liu, C.H. Tsai, B.C. Lan, Y.H. Lin, W.T. Chiang, C.T. Tsai, United Microelectronics Corporation, Hsin-Chu City, Taiwan

18.4 – 11:40 a.m.
Origin of Drivability Enhancement in Scaled pMOSFETs with 45^{o} Rotated <100> Channels, S. Saito, D. Hisamoto, Y. Kimura, N. Sugii, R. Tsuchiya, K. Torii, S. Kimura, Hitachi Ltd., Tokyo, Japan

12:05 p.m. Lunch

SESSION 19 – HONOLULU SUITE
Advanced CMOS Technology

Thursday, June 15, 10:25 a.m.
Chairpersons: M.-R. Lin, AMD
H. Wakabayashi, NEC Corp.

19.1 – 10:25 a.m.
High Performance Dual Metal Gate CMOS with High Mobility and Low Threshold Voltage Applicable to Bulk CMOS Technology, S. Yamaguchi, K. Tai, T. Hirano, T. Ando, S. Hiyama, J. Wang, Y. Hagimoto, Y. Nagahama, T. Kato, K. Nagano, M. Yamanaka, S. Terauchi, S. Kanda, R. Yamamoto, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, N. Nagashima, S. Kadomura, Sony Corporation, Kanagawa, Japan

19.2 – 10:50 a.m.
Low Power CMOS Featuring Dual Work Function FUSI on HfSiON and 17ps Inverter Delay, T. Hoffmann, A. Veloso, A. Lauwers, H. Yu, M. Van Dal, H. Tigelaar, T. Chiarella, C. Kerner, R. Mitsuhashi, I. Satoru, M. Niwa, A. Rothschild, B. Froment, J. Ramos, A. Nackaerts, S. Brus, C. Vrancken, P.P. Absil, M. Jurczak, J.A. Kittl, S. Biesemans, IMEC, Leuven, Belgium

19.3 – 11:15 a.m.
High-Performance Low Operation Power Transistor for 45nm Node Universal Applications, M. Shima, K. Okabe*, A. Yamaguchi*, T. Sakoda, K. Kawamura*, S. Pidin*, M. Okuno, T. Owada*, K. Sugimoto*, J. Ogura*, H. Kokura*, H. Morioka*, T. Watanabe*, T. Isome*, K. Okoshi*, T. Mori*, Y. Hayami*, H. Minakata, A. Hatada, Y. Shimamune, A. Katakami, H. Ota*, T. Sakuma*, T. Miyashita, K. Hosaka, H. Fukutome, N. Tamura, T. Aoyama, K. Sukegawa*, M. Nakaishi*, S. Fukuyama*, S. Nakai*, M. Kojima*, S. Sato, M. Miyajima*, K. Hashimoto*, T. Sugii, Fujitsu Laboratories Ltd., Tokyo, Japan, *Fujitsu Limited, Tokyo, Japan

19.4 – 11:40 a.m.
55nm CMOS Technology for Low Standby Power/Generic Applications Deploying the Combination of Gate Work Function Control by HfSiON and Stress-Induced Mobility Enhancement, H. Nakamura*, Y. Nakahara, N. Kimizuka, T. Abe, I. Yamamoto, T. Fukase, T. Nakayama, K. Taniguchi, K. Masuzaki*, K. Uejima*, T. Iwamoto*, T. Tatsumi*, K. Imai, NEC Electronics Corporation, Kanagawa, Japan, *NEC Corporation, Kanagawa, Japan

12:05 p.m. Lunch

SESSION 20 – TAPA I
Advanced High K Stacks

Thursday, June 15, 1:30 p.m.
Chairpersons: S. Deleonibus, CEA-LETI
T. Kuroi, Renesas Technology Corp.

20.1 – 1:30 p.m.
Poly-Si/AlN/HfSiO Stack for Ideal Threshold Voltage and Mobility in Sub-100 nm MOSFETs, K.L. Lee, M.M. Frank, V. Paruchuri, E. Cartier, B. Linder, N. Bojarczuk, X. Wang*, J. Rubino, M. Steen, P. Kozlowski, J. Newbury, E. Sikorski, P. Flaitz*, M. Gribelyuk*, P. Jamison, G. Singco, V. Narayanan, S. Zafar, S. Guha, P. Oldiges*, R. Jammy, M. Ieong, IBM Research Division, Yorktown Heights, NY, *IBM Systems and Technology Group, Hopewell Junction, NY

20.2 – 1:55 p.m.
Dual High-k Gate Dielectric Technology Using Selective AlO_x Etch (SAE) Process with Nitrogen and Fluorine Incorporation, H.-S. Jung, S.K. Han, H. Lim, Y.-S. Kim, M.J. Kim, M.Y. Yu, C.-K. Lee, M.S. Lee, Y.-S. You, Y. Chung*, S. Kim*, H.S. Baik*, J.-H. Lee, N.-I. Lee, H.-K. Kang, Samsung Electronics Co. Ltd., Kyunggi-Do, Korea, *Samsung Advanced Institute of Technology, Kyunggi-Do, Korea

20.3 – 2:20 p.m.
A Novel Remote Reactive Sink Layer Technique for the Control of N and O Concentrations in Metal/High-k Gate Stacks, Y. Akasaka[1], K. Shiraishi[2,3], N. Umezawa[3], O. Ogawa[1], T. Kasuya[1], T. Chikyow[3], F. Ootsuka[1], Y. Nara[1], K. Nakamura[1], [1]Semiconductor Leading Edge Technologies Inc., Ibaraki, Japan, [2]University of Tsukuba, Tsukuba, Japan, [3]National Institute for Materials Science

20.4 – 2:45 p.m.
Sub-1nm EOT $HfSi_x/HfO_2$ Gate Stack Using Novel Si Extrusion Process for High Performance Application, T. Ando, T. Hirano, K. Tai, S. Yamaguchi, T. Kato, Y. Hagimoto, K. Watanabe, R. Yamamoto, S. Kanda, K. Nagano, S. Terauchi, Y. Tateshita, Y. Tagawa, M. Saito, H. Iwamoto, S. Yoshida*, H. Watanabe*, N.Nagashima, S. Kadomura, Sony Corporation, Kanagawa, Japan, *Osaka University, Osaka, Japan

3:10 p.m. Break

SESSION 21 – HONOLULU SUITE
Front-End of Line Processing

Thursday, June 15, 1:30 p.m.
Chairpersons: K. Schruefer, Infineon
Y. Takao, Fujitsu Ltd.

21.1 – 1:30 p.m.
Enhanced Performance of PMOS MUGFET via Integration of Conformal Plasma-Doped Source/Drain Extensions, D. Lenoble, K. G. Anil, A. De Keersgieter, P. Eybens, N. Collaert, R. Rooyackers, S. Brus, P. Zimmerman, M. Goodwin, D. Vanhaeren, W. Vandervorst, S. Radovanov[1], L. Godet[1,2], C. Cardinaud[2], S. Biesemans, T. Skotnicki[3], M. Jurczak, IMEC, Leuven, Belgium, [1]VSEA, Gloucester, MA, [2]Nantes University, France, [3]STMicroelectronics, Alliance, France

21.2 – 1:55 p.m.
RTA-Driven Intra-Die Variations in Stage Delay, and Parametric Sensitivities for 65nm Technology, I. Ahsan, N. Zamdmer, O. Glushchenkov, R. Logan, E.J. Nowak[1], H. Kimura[2], J. Zimmerman[1], G. Berg, J. Herman, E. Maciejewski, A. Chan, A. Azuma[3], S. Deshpande, B. Dirahoui, G. Freeman, A. Gabor, M. Gribelyuk, S. Huang, M. Kumar, K. Miyamoto[3], D. Mocuta, A. Mahorowala, E. Leobandung, H. Utomo, B. Walsh, IBM Systems and Technology Group, Hopewell Junction, NY, [1]IBM Semiconductor Research and Development Center, Essex Junction, VT, [2]Sony Electronics Inc., Hopewell Junction, NY, [3]Toshiba America Electronic Component Inc., Hopewell Junction, NY

21.3 – 2:20 p.m.
Performance Enhancement in 45-nm Ni Fully-Silicided Gate/High-k CMIS using Substrate Ion Implantation, Y. Nishida, T. Yamashita, S. Yamanari, M. Higashi, K. Shiga, N. Murata, M. Mizutani, M. Inoue, S. Sakashita, K. Mori, J. Yugami, T. Hayashi, A. Shimizu, H. Oda, T. Eimori, O. Tsuchiya, Renesas Technology Corp., Hyogo, Japan

21.4 – 2:45 p.m.
Channel Stress Modulation and Pattern Loading Effect Minimization of Milli-Second Super Anneal for Sub-65nm High Performance SiGe CMOS, C.-H. Chen, C.F. Nieh, D.W. Lin, K.C. Ku, J.C. Sheu, M.H. Yu, L.T. Wang, H.H. Lin, H. Chang, T.L. Lee, K. Goto, C.H. Diaz, S.C. Chen, M.S. Liang, Taiwan Semicoductor Manufacturing Co. Ltd.

3:10 p.m. Break

SESSION 22 – TAPA I
Novel Gate Stacks Engineering and Characterization

Thursday, June 15, 3:25 p.m.
Chairpersons: D. Gravesteijn, Philips Research Leuven
C. C. Wu, TSMC

22.1 – 3:25 p.m.
Novel Stack-SIN Gate Dielectrics for High Performance 30 nm CMOS for 45 nm Node with Uniaxial Strained Silicon, H. Ohta, M. Hori, M. Shima*, H. Mori, Y. Shimamune*, T. Sakuma, A. Hatada*, A. Katakami*, Y. Kim, K. Kawamura, T. Owada, H. Morioka, T. Watanabe, Y. Hayami, J. Ogura, N. Tamura*, M. Kojima, K. Hashimoto, Fujitsu Limited, Tokyo, Japan, *Fujitsu Laboratories Ltd., Tokyo, Japan

22.2 – 3:50 p.m.
Band-Edge High-Performance High-*k*/Metal Gate n-MOSFETs using Cap Layers Containing Group IIA and IIIB Elements with Gate-First Processing for 45 nm and Beyond, V. Narayanan, V.K. Paruchuri, N.A. Bojarczuk, B.P. Linder, B. Doris, Y.H. Kim, S. Zafar, J. Stathis, S. Brown, J. Arnold, M. Copel, M. Steen, E. Cartier, A. Callegari, P. Jamison, D.L. Lacey, Y. Wang*, P.E. Batson, P. Ronsheim*, R. Jammy, M.P. Chudzik, M. Ieong, S. Guha, G. Shahidi, T.C. Chen, IBM Semiconductor Research and Development Center, Yorktown Heights, NY, *IBM Systems and Technology Division, Hopewell Junction, NY

22.3 – 4:15 p.m.
Two Different Mechanisms for Determining Effective Work Function ($\Phi_{m,eff}$) on High-k - Physical Understanding and Wider Tunability of $\Phi_{m,eff}$ -, M. Kadoshima, A. Ogawa, H. Ota*, M. Ikeda, M. Takahashi, H. Satake, T. Nabatame, A. Toriumi*,[#], MIRAI-ASET, Ibaraki, Japan, *MIRAI-ASRC, Tsukuba, Japan, [#]The University of Tokyo, Tokyo, Japan

22.4 – 4:40 p.m.
Sub-1Å-Resolution Analysis and Physical Understanding of Gate/Insulator Interfacial Region in Scaled-T_{inv} High-k Gate Stacks, M. Saitoh, Y. Tsuchiya, Y. Kamimuta, T. Saito, K. Sekine, T. Kobayashi, T. Aoyama, M. Koyama, A. Nishiyama, Toshiba Corporation, Yokohama, Japan

SESSION 23 – HONOLULU SUITE
Advanced Source/Drain Engineering

Thursday, June 15, 3:25 p.m.
Chairpersons: M. Mirabedini, LSI Logic Corp.
H. Wakabayashi, NEC Corp.

23.1 – 3:25 p.m.
Novel Approach to Reduce Source/Drain Series Resistance in High Performance CMOS Devices Using Self-Aligned CoWP Process for 45nm Node UTSOI Transistors with 20nm Gate Length, J. Pan, A. Topol*, I. Shao*, D. Singh* Z. Ren*, C.-Y. Sung*, M. Ieong*, J. Pellerin, J. Iacoponi, M.-R. Lin, AMD Corporation, Hopewell Junction, NY, *IBM T. J. Watson Research Center, Yorktown Heights, NY

23.2 – 3:50 p.m.
Advanced Junction Profile Engineering Featuring Laser Spike Annealing and Co-implantation for Sub-30-nm Strained CMOS Devices, T. Yamamoto, T. Kubo, T. Sukegawa, K. Hashimoto, M. Kase, Fujitsu Ltd., Tokyo, Japan

23.3 – 4:15 p.m.
Unique Ultra Shallow Junction Scheme with Conventional Activation Process, C.H. Tsai, B.C. Lan, Y.H. Lin, W.T. Chiang, T.Y. Chang, P.W. Liu, J.W. Pan, Y.C. Liu, J.L. Tsai, T.F. Chen, C.T. Tsai, United Microelectronics Corporation, Hsin-Chu City, Taiwan

23.4 – 4:40 p.m.
A Raised Source/Drain Extension pFET on Si (110) Realized by In-situ Doped Selective Epitaxy Technology, J. Wang, Y. Kikuchi, Y. Tateshita, T. Kato, T. Kataoka, T. Hirano, K. Nagano, T. Ikuta, Y. Miyanami, S. Fujita, S. Hiyama, R. Yamamoto, S. Kanda, S. Yamakawa, T. Kimura, K. Kugimiya, N. Yamagishi, Y. Tagawa, Y. Kamide, H. Iwamoto, T. Ohno, M. Saito, S. Kadomura, N. Nagashima, Sony Corporation, Kanagawa, Japan

GENERAL INFORMATION

SCOPE OF SYMPOSIUM: The Symposium on VLSI Technology covers all aspects of VLSI technology, such as: new concepts and breakthroughs in VLSI devices and processes; new functional devices including quantum effect devices with possible VLSI implementation; materials innovation for MOSFET and interconnect in VLSI; advanced lithography and fine patterning technologies for high density VLSI; process/device modeling of VLSI devices; packaging and reliability of VLSI devices; theories and fundamentals related to the above devices; and new concepts and technologies for VLSI manufacturing.

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Circ Symposium	$500	$550	$250
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*(**This year the Circuits Short Course is comprised of two programs, Analog and Digital. The cost of the short course includes both programs and attendees will receive one book for both programs. Attendees will be able to move back and forth between the two programs.)*

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Symposium on VLSI Technology

Sunday, June 11	5:00 pm - 8:00 pm
Monday, June 12	8:00 am - 5:00 pm
Tuesday, June 13	7:30 am - 5:30 pm
Wednesday, June 14	7:30 am - 5:00 pm
Thursday, June 15	7:30 am - 5:00 pm

Symposium on VLSI Circuits

Wednesday, June 14	7:30 am - 5:00 pm
Thursday, June 15	7:30 am - 5:00 pm
Friday, June 16	7:30 am - 5:00 pm
Saturday, June 17	7:30 am - 12:00 noon

VLSI TECHNOLOGY SYMPOSIUM RECEPTION: A reception will be held on Monday, June 12 from 6:00 pm to 8:00 pm on the Lagoon Green.

VLSI TECHNOLOGY SYMPOSIUM BANQUET: The 2006 Symposium on VLSI Technology Banquet will be held on Tuesday, June 13 on the Lagoon Green from 7:00 pm to 9:00 pm. Banquet tickets for accompanying guests can be purchased at the Registration desk in the Palace Lounge Lobby.

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