SESSION 1 – TAPA II
Plenary Session

Wednesday, June 18, 8:25 a.m.
Chairpersons: K. Nakamura, Analog Devices Inc.
M. Mizuno, NEC Corporation

8:25 a.m. **Welcome and Opening Remarks**
S. Kosonocky, AMD
K. Yano, Hitachi Ltd.

1.1 – 8:40 a.m.
Next Generation Micro-Power Systems
A.P. Chandrakasan, D.C. Daly, J. Kwong, Y.K. Ramadass,
Massachusetts Institute of Technology

Emerging microsystems such as portable and implantable medical electronics, wireless microsensors and next-generation battery-operated multimedia devices demand a dramatic reduction in energy consumption. The ultimate goal is to power these devices using energy harvesting techniques such as vibration-to-electric conversion or through wireless power transmission. A major opportunity to reduce the power dissipation of digital circuits is to scale supply voltages to 0.5V and below. The challenges associated with ultra-low-voltage design in scaled technologies will be presented. This includes variation-aware design for logic and SRAM circuits, efficient DC-DC converters for ultra-low-voltage delivery, and algorithm structuring to support extreme parallelism. Micro-power analog and RF circuits require the use of application-specific structures as well as digital and variation-aware architectures to leverage process scaling.

1.2 – 9:25 a.m.
Power-Efficient Heterogeneous Parallelism for Digital Convergence
K. Uchiyama, Hitachi, Ltd.

For embedded systems in the digital-convergence era, various functions such as communication, security, audio, video, and recognition, are required in a single device. However, improving the speed of an embedded LSI in the system is difficult because of the significantly increasing power-consumption problems. Heterogeneous parallelism on an SoC has been studied to solve these problems. A power-thrifty architecture, which combines embedded CPUs and special processing cores such as dynamic reconfigurable processors, has been proposed targeting a superior performance per power ratio and functional flexibility. From the viewpoint of programming, a parallelizing compiler and an Application Program Interface (API) have been developed that are suitable for heterogeneous parallelism. The evaluation results of various applications tested using prototype chips and programs will also be discuss ed.