SESSION 13 – TAPA II
Low Power Memory and Interface Techniques

Thursday, June 19, 3:25 p.m.
Chairpersons: O. Jungroth, Intel Corporation
K. Kajigaya, Elpida Memory, Inc.

13.1 – 3:25 p.m.
A Fully Logic-Process-Compatible, 3-Transistor, SESO-memory Cell Featuring 0.1-FIT/Mb Soft Error, 100-MHz Random Cycle, and 100-ms Retention, N. Kameshiro, T. Watanabe, T. Ishii, T. Mine, T. Sano*, H. Ibe, S. Akiyama, K. Yanagisawa**, T. Ipposhi**, T. Iwamatsu**, Y. Takahashi**, Hitachi Ltd., *Renesas Northern Japan Semiconductor Inc., **Renesas Technology Corp., Japan

A 1-kb memory-cell array composed of single-electron shut-off (SESO) cells was fabricated with the 90-nm logic process for the first time. It features a 0.1-FIT/Mb soft error, 100-MHz random cycle, and 100-ms retention. In addition to a logic-compatible cell structure and a write-data caching scheme, a backup latch circuit with SESO transistors for logic application was also proposed.

13.2 – 3:50 p.m.
Novel Co-design of NAND Flash Memory and NAND Flash Controller Circuits for Sub-30nm Low-Power High-Speed Solid-State Drives (SSD), K. Takeuchi, University of Tokyo, Japan

Three new circuit technologies, selective bit-line precharge scheme, advanced source-line programming, and intelligent interleaving are proposed. By co-designing NAND flash memory and NAND controller circuits, both NAND and the NAND controller are best optimized. The operation current of the NAND flash memory decreases by 60% and 2.5 times as many NAND chips in SSD can operate simultaneously. At sub-30nm generation, the SSD performance improves by 150% without a cost penalty or circuit noise.

13.3 – 4:15 p.m.
A 16Gb/s/link, 64GB/s Bidirectional Asymmetric Memory Interface Cell, K. Chang, H. Lee, J.-H. Chun, T. Wu, T.J. Chin, K. Kaviani, J. Shen, X. Shi, W. Beyene, Y. Frans, B. Leibowitz, N. Nguyen, F. Quan, J. Zerbe, R. Perego, F. Assaderaghi, Rambus Inc., USA

An asymmetric memory interface cell with 32 bidirectional data and four unidirectional request links operating at 16Gb/s per link is implemented in TSMC 65nm CMOS technology. Timing adjustment and equalization circuits for both memory read and write are on the controller to reduce memory cost. Each link operates at a maximum rate of 16Gb/s with comparable margins in both directions at a BER of 10-12. The measured energy efficiency for the cell is 13mW/Gb/s.

13.4 – 4:40 p.m.
A 16-Gb/s Differential I/O Cell with 380fs RJ in an Emulated 40nm DRAM Process, N. Nguyen, Y. Frans, B. Leibowitz, S. Li, R. Navid, M. Aleksic, F. Lee, F. Quan, J. Zerbe, R. Perego, F. Assaderaghi, Rambus Inc., USA

This paper describes a 16-Gb/s differential bidirectional I/O transceiver cell in an emulated 40nm DRAM process. The transceiver implements several techniques to achieve low jitter despite the slow process and constrained power consumption. The transceiver has measured random jitter of 380fs rms at the transmitter output and BER < 10-14 while consuming 8mW/Gb/s.