SESSION 17 – TAPA I
High Speed Timing Circuits

Friday, June 20, 10:10 a.m.
Chairpersons: S. Tam, Intel Corporation
J.-Y. Sim, POSTECH

17.1 – 10:10 a.m.
Time-to-Digital Converter with Vernier Delay Mismatch Compensation for High Resolution On-Die Clock Jitter Measurement, T. Hashimoto, H. Yamazaki, A. Muramatsu, T. Sato, A. Inoue, Fujitsu Laboratories Limited, Japan

A time-to-digital converter (TDC) utilizing a vernier delay line (VDL) technique has relatively large timing errors when the mismatch of the vernier delay is large. In order to overcome this problem, we propose a technique for compensating the vernier delay mismatch using multiple ring oscillation measurements of VDL. We verified it using an on-die jitter measurement circuit implemented in 90nm CMOS technology and 0.880ps timing resolution was obtained experimentally.

17.2 – 10:35 a.m.
In-Situ Jitter Tolerance Measurement Technique for Serial I/O, J. Jaussi, G. Balamurugan, J. Kennedy, F. O'Mahony, M. Mansuri, R. Mooney, B. Casper, U.-K. Moon*, Intel Corporation, *Oregon State University, USA

A 10.2-12.5Gb/s CDR incorporating an on-die jitter modulation circuit that enables in-situ jitter tolerance testing is demonstrated in 65nm CMOS. Sinusoidal jitter is introduced into the CDR loop by modulating the control voltage of the LC-VCO and is programmable in amplitude and frequency. The modulation frequency range is 340kHz-104MHz with modulation amplitudes up to 44UIpp. The on-die jitter tolerance measurements correlate to conventional external jitter tolerance results within 10% across a 0.73-23.5MHz range.

17.3 – 11:00 a.m.
Phase Correction of a Resonant Clocking System Using Resonant Interpolators, L.-M. Lee, C.-K.K. Yang, University of California, Los Angeles, USA

Large static phase errors result from injection-locked LC clock buffers due to slight frequency mismatch between the input frequency and the tank's resonant frequency. The paper demonstrates a technique embedding a resonant interpolator into the clock buffer to correct the phase error without additional buffer elements. The test chip is fabricated in a 0.13µm digital CMOS technology. Measured DNL of the resonant interpolator is <0.6LSB even with quadrature inputs and phase error <1ps is achieved.

17.4 – 11:25 a.m.
A Multi Standard 1.5 to 10Gb/s Latch-Based 3-Tap DFE Receiver with a SSC Tolerant CDR for Serial Backplane Communication, M. Pozzoni, S. Erba, P. Viola, M. Pisati, E. Depaoli, D. Sanzogni, R. Brama**, D. Baldi, M. Repossi, F. Svelto*, STMicroelectronics, *Universita degli Studi di Pavia, **Universita di Modena e Reggio Emilia, Italy

A 1.5 to 10Gb/s SATA/SAS/FC receiver in 65nm CMOS is presented. It is based on an adaptive 3-tap latch-based DFE data recovery with self-aligning capability and on an early-late digital clock recovery capable of SSC tracking. Extensive digital features allow self-calibration and eye analysis. The macro measures 0.3mm2 and consumes 140mA from 1V at 8.5Gb/s.