SESSION 18 – TAPA II
Oversampled Data Converters

Friday, June 20, 10:10 a.m.
Chairpersons: J. Gealow, MediaTek Wireless, Inc.
M. Ito, Renesas Technology Corporation

18.1 – 10:10 a.m.
A 1.3-mW per-Channel 103-dB SNR Stereo Audio DAC with Class-D Head-Phones Amplifier in 65nm CMOS, Y.-H. Lee, C.-K. Seok, B.-J. Kim, S.-B. You, W.-S. Yeum, H.-J. Park, Y.-H. Jun, B.-S. Kong*, J.-W. Kim, Samsung Electronics, *Sungkyunkwan University, Korea

The stereo audio DAC with novel single-ended class-D amplifier achieving a 103-dB SNR is fully integrated in a 65nm CMOS technology. Novel asymmetric pulse-width modulation (PWM) is applied to minimize switching noise and nonlinearity in the class-D amplifier. The adjustable delta-sigma modulator is also used to suppress supply-voltage modulation. All the functions needed for portable audio playback are implemented in a 0.53-mm2 area dissipating only 1.3-mW per channel from a 2.5-V supply.

18.2 – 10:35 a.m.
A 0.7-V 100-dB 870-µW Digital Audio Σ Δ Modulator, H. Park, K. Nam, D. Su, K. Vleugels, B. Wooley, Stanford University, USA

A high-precision, low-voltage, low-power ∑Δ modulator has been designed using a delayed input feedforward architecture and a tracking multi-bit quantizer employing a single comparator. A 0.18-µm CMOS experimental prototype achieves 100 dB of dynamic range, 100-dB peak SNR and 95-dB peak SNDR for a signal bandwidth of 25 kHz, while consuming only 870 µW of total power from a 0.7-V supply at a 5-MHz sampling rate.

18.3 – 11:00 a.m.
A 2.1mW/3.2mW Delay-Compensated GSM/WCDMA Σ Δ Analog-Digital Converter, M. Vadipour, C. Chen, A. Yazdi, M. Nariman, T. Li, P. Kilcoyne, H. Darabi, Broadcom Corporation, USA

A technique to compensate for the harmful excess loop delay in a continuous time ∑Δ analog-digital converter is presented. With no extra power consumption or area penalty the technique is suitable for variety of applications employing continuous time ∑Δ analog-digital converters. This work presents a dual mode ∑Δ ADC for GSM/WCDMA applications with DR of 86dB/63dB for 100KHz/1.92MHz in a 65nm CMOS technology with power consumption of 2.1mW/3.2mW.

18.4 – 11:25 a.m.
A 14b 23MS/s 48mW Resetting Σ Δ ADC with 87dB SFDR 11.7b ENOB & 0.5mm^2 Area, C. Lee, M. Flynn, University of Michigan, USA

A 14b 23MS/s ADC that pipelines a 2nd order resetting SD modulator with a 10b cyclic ADC and requires no front-end S/H is presented. The architecture uses a resetting ∑Δ modulator at the front-end for accuracy and a cyclic ADC at the back-end for residual error quantization. This calibration-free ADC achieves no missing codes, 87dB SFDR and 11.7b ENOB. Fabricated in 0.18µm CMOS with a core area of 0.5mm2, it consumes 48mW from a 2V supply.