SESSION 20 – TAPA II
High Speed Transceivers

Friday, June 20, 1:30 p.m.
Chairpersons: J. Savoj, Qualcomm
J. Lee, National Taiwan University

20.1 – 1:30 p.m.
A 40-Gb/s Transceiver in 0.13-µm CMOS Technology, J.-K. Kim, J. Kim**, G. Kim*, H. Chi, D.-K. Jeong, Seoul National University, Korea, *Silicon Image, **Rambus Inc., USA

A fully integrated 40-Gb/s transceiver is implemented in a 0.13-µm CMOS. This paper describes the challenges in designing a 20-GHz sampler, a 20-GHz quadrature LC-VCO, a 20-GHz bang-bang phase detector, and a 40-Gb/s equalizer. The transceiver dissipates 3.6W from a 1.45-V supply. With the equalizer on, the transmit jitter of the 39-Gb/s PRBS data after the package and board traces is 1.85psrms and the recovered clock jitter is 1.77psrms. The measured BER is <1.0E-14.

20.2 – 1:55 p.m.
A 7.5Gb/s Transmitter with Self-Adaptive FIR, D. Tonietto, J. Hogeboon, E. Bensoudane, S. Sadeghi, H. Khor, P. Krotnev, STMicroelectronics, Canada

This paper presents an adaptation method for transmit multi-tap FIR based on exploration of the receive eye at the far end receiver. This method does not require back-channel or coding overhead and does not involve any proprietary functionality in the far-end SerDes. The proposed method was proven in a CMOS 65n SerDes over a variety of copper media for data-rates up to 9.4 Gbps.

20.3 – 2:20 p.m.
A TeraBit/s-Throughput, SerDes-Based Interface for a Third-Generation 16 Core 32 Thread Chip-Multithreading SPARC Processor, J. Nasrullah, A. Amin, W. Ahmad, Z. Qin, Z. Mushtaq, O. Javed, J. Yoon, L. Chua, D. Huang, B. Huang, M. Vichare, K. Ho, M. Rashid, Sun Microsystems, USA

Third-generation 16 core 32 thread chip-multithreading SPARC processor interface has 1.1Tbps I/O throughput with 112 Tx/176 Rx SerDes channels in 46mm2. Individual links run at BER of 1E-12 on FR4 PCBs at 4.08-0.5Gbps full-half rate, and 18mW/ch/Gbps at 2.67Gbps. Each link has linear equalization, 15 deemphasis and 8 output-swing control settings, and latency of 8UI in Rx and 14-16UI in Tx.

20.4 – 2:45 p.m.
A 21-Channel 8Gb/s Transceiver Macro with 3.6ns Latency in 90nm CMOS for 80cm Backplane Communication, A. Hayashi, M. Kuwata, K. Suzuki, T. Muto, M. Tsuge, K. Nagashima, D. Hamano, T. Usugi, K. Nakajima, M. Ogihara, N. Mikami*, K. Watanabe, Hitachi Ltd., *Hitachi ULSI Systems, Japan

A 21-Channel 8Gb/s transceiver is implemented in a 90nm CMOS technology. 168Gb/s uncoded data transmission with 3.6ns latency is achieved with 4-tap FFE, receiver equalization, jitter tolerant CDR and low jitter PLL. Measured bathtub plots for 80cm FR-4 backplane indicate BER<10-15 with 0.11UI phase margin at the nominal power consumption of 160mW/ch.