SESSION 5 – TAPA II
SRAM Variability

Wednesday, June 18, 3:25 p.m.
Chairpersons: A. Bhavnagarwala, IBM TJ Watson Research Ctr.
T. Sekiguchi, Hitachi, Ltd.

5.1 – 3:25 p.m.
Large-Scale Read/Write Margin Measurement in 45nm CMOS SRAM Arrays, Z. Guo, A. Carlson, L.-T. Pang, K. Duong, T.-J. King Liu, B. Nikolic, University of California, Berkeley, USA

Distributions of read and write noise margins in large CMOS SRAM arrays are investigated by directly measuring the bit-line current during bitline / wordline (write) or cell supply (read) voltage sweep in a 768Kb 7M1P 45nm CMOS SRAM test-chip. Good correlation between the margins estimates through bitline current measurements and the conventional DC margin measurements in small on-chip SRAM macros with wired-out storage nodes is demonstrated.

5.2 – 3:50 p.m.
Characterization of Bit Transistors in a Functional SRAM, X. Deng, W.K. Loh, B. Pious, T.W. Houston, L. Liu, B. Khan, D. Corum, J. Raval, J. Gertas, F.-Y. Rousey, J. Steck, C. Suwannakinthorn, R. McKee, Texas Instruments, USA

A direct bit transistor access (DBTA) scheme is proposed and implemented in 8Mb SRAMs at 65nm and 45nm nodes. It allows, for the first time, characterization of each bit transistor in a functional SRAM. It thus enables (a) collection of transistor data across bit arrays, (b) collection of massive data for statistical analysis such as on transistor mismatch and NBTI Vt drift, and (c) collection of data for fast failure analysis. Measured data are presented.

5.3 – 4:15 p.m
A 0.7V Single-Supply SRAM With 0.495um^2 Cell In 65nm Technology Utilizing Self-Write-Back Sense Amplifier And Cascaded Bit Line Scheme, K. Kushida, A. Suzuki, G. Fukano, A. Kawasumi, O. Hirabayashi, Y. Takeyama, T. Sasaki, A. Katayama, Y. Fujimura,. T. Yabe, Toshiba Corporation, Japan

A novel SRAM architecture with a high density cell in low supply voltage operation is proposed. A self-write-back sense amplifier realizes cell failure rate improvement by more than two orders of magnitude at 0.6V. A cascaded bit line scheme saves additional process cost for hierarchical bit line layer. A test chip with 256kb SRAM utilizing 0.495µm2 cell in 65nm CMOS technology demonstrated 0.7V single supply operation.

5.4 – 4:40 p.m.
PVT-Variations and Supply-Noise Tolerant 45nm Dense Cache Arrays with Diffusion-Notch-Free (DNF) 6T SRAM Cells and Dynamic Multi-Vcc Circuits, M. Khellah, N.S. Kim, Y. Ye, D. Somasekhar, T. Karnik, N. Borkar, F. Hamzaoglu, T. Coan, Y. Wang, K. Zhang, C. Webb, V. De, Intel, USA

PVT-tolerant and supply noise tracking word-line under-drive circuit, PMOS pass device, and dynamic voltage collapse enable read and write stable Diffusion-Notch-Free (DNF) 6T SRAM cells. Measurements from a 45-nm test-chip show 26X reduction in number of single bit failures using those schemes.