SESSION 6 – TAPA III
**Wireline Signal Conditioning**

Wednesday, June 18, 3:25 p.m.
Chairpersons: J. Wieser, National Semiconductor
H. Yamada, Oki Electric Industry Co., Ltd.

**6.1 – 3:25 p.m.**
**A 70dB MTPR Integrated Programmable Gain/Bandwidth 4th-Order Chebyshev Highpass Filter for ADSL/VDSL Receivers in 65nm CMOS,** F. Lin, X. Yu, S. Ranganathan, T. Kwan, Broadcom Corporation, USA

This paper presents a 4th-order Chebyshev HPF in 65nm CMOS process with programmable gain and corner frequency to support ADSL and 5/6 band VDSL applications. The HPF improves noise performance by applying capacitive feedback and feedforward in the filter. It achieves a 70dB MTPR and -161dBm/Hz (2.8nV/ÖtHz) input referred noise for ADSL mode. An IM3 of -80dBc at 10MHz is measured for VDSL mode.

**6.2 – 3:50 p.m.**
**A 40Gb/s Low-Power Analog Equalizer in 0.13µm CMOS Technology,** J.-H. Lu, K.-H. Chen, S.-I. Liu, National Taiwan Univ., Taiwan

A 40Gb/s low-power analog equalizer has been realized in 0.13µm CMOS technology. To achieve a peaking gain of 10dB at 20GHz and low power dissipation, an inductive feedback stage is proposed. This inductive feedback stage consumes 3.6mW from a 1.2V supply and the whole equalizer consumes 14.4mW. The chip occupies 0.57×0.44mm2. For a 40Gb/s PRBS of 27-1, the measured BER is less than 10-12 and the measured maximum peak-to-peak jitter is 12.6ps.

**6.3 – 4:15 p.m.**
**A Merged CMOS Digital Near-End Crosstalk Canceller and Analog Equalizer for Multi-Lane Serial-Link Receivers,** J.-H. Lu, K.-H. Chen, A.-M. Lee*, T.-Y. Wu*, S.-I. Liu, National Taiwan University, *Realtek Semiconductor Corp., Taiwan

A digital near-end crosstalk (NEXT) canceller merged with an analog equalizer for multi-lane serial-link receivers has been realized in 0.13µm CMOS technology. With the proposed sign-sign block least-mean-square (SSB-LMS) circuit, a 5Gb/s PRBS of 231-1 suffered from both the channel loss and NEXT for 10-inch FR4 traces is successfully equalized. The measured BER is 10-12 and the measured maximum peak-to-peak jitter is 49.7ps. This chip occupies 0.56×0.76mm2 and consumes 177mW including buffers from a 1.2V supply.

**6.4 – 4:40 p.m.**
**A 12-Gb/s 11-mW Half-Rate Sampled 5-Tap Decision Feedback Equalizer with Current-Integrating Summers in 45-nm SOI CMOS Technology,** T. Dickson, J. Bulzacchelli, D. Friedman, IBM T.J. Watson Res. Ctr, USA

The design and experimental results of a low-power, low-area 5-tap DFE implemented in 45-nm SOI CMOS technology are reported. The DFE employs a low-power current-integrating summer with sampling front-end, which eliminates systematic loss inherent in conventional integrating serial receivers. The use of a direct-feedback architecture and CMOS-style rail-to-rail clocking achieves further power and area savings. The 5-tap DFE core occupies 73µm x 50µm and consumes 11 mW from a 1V supply when equalizing 12-Gb/s data passed over a 30" channel with 15dB of loss at 6 GHz.